MODEL 451
Microwave Pulse Counter

EIP Microwave, Inc
2731 North First Street, San Jose, CA 95134

TEL (408) 946-5700
TWX 910-338-0155

Manual Part Number: 5580010
Manual printed in U.S.A. – OCT 1978

CCN 1004

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF TABLES

LIST OF ILLUSTRATIONS

NOTE: The following figures include the Component Locator, Circuit Description, and Schematic Diagram for the PCB assemblies in this counter. All related sheets for a particular assembly have the same figure number. Page numbers given below indicate the beginning page of a particular assembly.

SECTION 1

GENERAL INFORMATION & SPECIFICATIONS

1-1. DESCRIPTION

1-2. The EIP Model 451 Microwave Pulse Counter automatically and directly measures the frequency of pulse modulated microwave signals between 300 MHz - 18 GHz. Pulse widths can be as narrow as 100 nanoseconds, with no minimum or maximum pulse repetition frequency limits.

1-3. The 451 also measures the frequency of CW microwave signals, and carrier signals with FM modulation up to 40 MHz peak-to-peak deviation at 10 MHz modulation rates. No manual switching is required to measure CW or pulsed frequencies — the counter will automatically measure either type of signal. Sensitivity is -10 dBm to 10 GHz; -5 dBm to 18 GHz. A built-in limiter provides overload protection of up to 1 watt peak from 925 MHz - 18 GHz.

1-4. All front panel controls except SAMPLE RATE are externally programmable. One input to the counter (Band B) accepts signals over the range of 925 MHz - 18 GHz. Option P2 provides a second input (Band A) to cover the range of 300 MHz - 950 MHz.

1-5. The display on the 451 Counter provides a direct readout of the measured frequency over the entire operating range of the counter with 10 kHz resolution. The counter also includes automatic suppression of leading zeros, except during a no signal input condition.

1-6. The frequency readout of the 451 is displayed in a fixed position format that is conveniently sectionalized in GHz and MHz. Gate times are 100 µs and 1 ms.

1-7. For applications where less resolution is required, pushbutton display blanking (RESOLUTION) is provided to simplify the readout.

1-8. To assure trouble-free performance, the 451 Pulse Counter is completely solid-state. For ease of repair and maintenance, the major portion of the counter circuitry is contained on plug-in printed circuit boards or in easily removed modules. Special test points allow monitoring of critical circuit functions.

1-9. INSTRUMENT IDENTIFICATION

1-10. The 451 Pulse Counter is identified by two number sets: the Model and Configuration Control Number (e.g: 451-CCN1001), and a specific Serial Number (e.g: 12345). Both sets of numbers should be mentioned in any correspondence or parts orders relating to the counter.

1-11. SPECIFICATIONS

1-12. Model 451 Microwave Pulse Counter specifications are given in Table 1-1.

GENERAL SPECIFICATIONS

Frequency Range: Band A: Band B:	**300 MHz to 950** MHz (Option P2) **925 MHz to 18** GHz
Pulse Characteristics: Pulse width: Pulse repetition freq.:	 100 nsec min. (measured at 3 dB points) Minimum-50 Hz normal, 0 Hz rear panel selected, Maximum - No limit
Accuracy: CW or pulses >100 μsec: Pulse <100 μsec:	 Time base accuracy ±1 count Time base accuracy ± averaging error ± gate error
Averaging error (kHz rms): 100 μs Gate: 1 ms Gate: Gate error (max.):	Band A / Band B $\frac{200}{\sqrt{PW-.03}}$ / $\frac{100}{\sqrt{PW-.03}}$ $\frac{60}{\sqrt{PW-.03}}$ / $\frac{30}{\sqrt{PW-.03}}$ $\pm\frac{100\ kHz}{PW-.03}$ / $\pm\frac{40\ kHz}{PW-.03}$ PW = pulse width in μs.
Time Base:	Standard / Option P1
Oscillator Type:	Room Temperature Crystal / Temperature Compensated Crystal (TCXO)
Crystal frequency:	10 MHz
Stability: Aging rate: Temperature: (0-50°C)	 $<\lvert 3\times10^{-7}\rvert$ /mon. $<\lvert 3\times10^{-5}\rvert$ / $<\lvert 2\times10^{-6}\rvert$
Line voltage:	±10% change produces frequency shift $<\lvert 1\times10^{-7}\rvert$
Warm up time:	None required

Sensitivity: Band A (Opt. P2): Band B:	 300 to 950 MHz -10 dBm peak 925 MHz to 10 GHz -10 dBm peak 10 GHz to 18 GHz -5 dBm peak
FM Tolerance Band B (minimum):	CW: 40 MHz p-p deviation for mod. rates DC-10 MHz. PULSE (w/o Input Inhibit): 20 MHz max. freq. shift across pulse. FREQUENCY PROFILE (using Input Inhibit): 20 MHz max. freq. shift during input inhibit pulse.
Maximum Input Level (peak): Band A: 300 to 950 MHz (Opt. P2) Band B: 925 MHz to 18 GHz	Operating / Burnout Level +10 dBm / +27 dBm +10 dBm / +30 dBm
Input Impedance: Connector:	Band A (Opt. P2) / Band B 50 Ω nom. / 50 Ω nom. BNC / Type N precision
Measurement Speed (Band B Only): Acquisition Time: PRF >100 Hz: PRF <100 Hz:	 100 msec + 50 msec/GHz 100 msec + $\frac{5}{PRF}$ sec/GHz
Reading Time Band B (sec): 100 μs Gate: 1 ms Gate:	Band A / Band B $\frac{400}{(PW)(PRF)}$ / $\frac{100}{(PW)(PRF)}$ $\frac{4000}{(PW)(PRF)}$ / $\frac{1000}{(PW)(PRF)}$ PW = pulse width (μsec) PRF = pulse repetition frequency (Hz)
Display:	7 digit LED with fixed decimal point. Leading zero suppression.
Resolution:	10 kHz, 100 kHz, 1 MHz
Power:	100/120/220/240 VAC ±10%, 50-60 Hz, 100 watts nominal.

GENERAL SPECS. CONT'D.

Operating Temperature:	0 to 50°C
Weight:	Net 30 lbs. Shipping 35 lbs.
Dimensions:	3.5" high and 16.75" wide and 19" deep
Accessories Furnished:	8 foot power cord and instruction manual
Accessories Available:	Model 400 Delay Generator. Carrying Case. P/N 5700001 Rack Mtg. Kit. P/N 2010008

TABLE 1-1. SPECIFICATIONS - 451 MICROWAVE PULSE COUNTER

SECTION 1

GENERAL INFORMATION & SPECIFICATIONS

1-1. DESCRIPTION

1-2. The EIP Model 451 Microwave Pulse Counter automatically and directly measures the frequency of pulse modulated microwave signals between 300 MHz - 18 GHz. Pulse widths can be as narrow as 100 nanoseconds, with no minimum or maximum pulse repetition frequency limits.

1-3. The 451 also measures the frequency of CW microwave signals, and carrier signals with FM modulation up to 40 MHz peak-to-peak deviation at 10 MHz modulation rates. No manual switching is required to measure CW or pulsed frequencies — the counter will automatically measure either type of signal. Sensitivity is -10 dBm to 10 GHz; -5 dBm to 18 GHz. A built-in limiter provides overload protection of up to 1 watt peak from 925 MHz - 18 GHz.

1-4. All front panel controls except SAMPLE RATE are externally programmable. One input to the counter (Band B) accepts signals over the range of 925 MHz - 18 GHz. Option P2 provides a second input (Band A) to cover the range of 300 MHz - 950 MHz.

1-5. The display on the 451 Counter provides a direct readout of the measured frequency over the entire operating range of the counter with 10 kHz resolution. The counter also includes automatic suppression of leading zeros, except during a no signal input condition.

1-6. The frequency readout of the 451 is displayed in a fixed position format that is conveniently sectionalized in GHz and MHz. Gate times are 100 µs and 1 ms.

1-7. For applications where less resolution is required, pushbutton display blanking (RESOLUTION) is provided to simplify the readout.

1-8. To assure trouble-free performance, the 451 Pulse Counter is completely solid-state. For ease of repair and maintenance, the major portion of the counter circuitry is contained on plug-in printed circuit boards or in easily removed modules. Special test points allow monitoring of critical circuit functions.

1-9. INSTRUMENT IDENTIFICATION

1-10. The 451 Pulse Counter is identified by two number sets: the Model and Configuration Control Number (e.g: 451-CCN1001), and a specific Serial Number (e.g: 12345). Both sets of numbers should be mentioned in any correspondence or parts orders relating to the counter.

1-11. SPECIFICATIONS

1-12. Model 451 Microwave Pulse Counter specifications are given in Table 1-1.

GENERAL SPECIFICATIONS

Frequency Range: Band A: Band B:	**300 MHz to 950** MHz (Option P2) **925 MHz to 18** GHz
Pulse Characteristics: Pulse width: Pulse repetition freq.:	 100 nsec min. (measured at 3 dB points) Minimum-50 Hz normal, 0 Hz rear panel selected, Maximum - No limit
Accuracy: CW or pulses >100 μsec: Pulse <100 μsec: Averaging error (kHz rms): 100 μs Gate: 1 ms Gate: Gate error (max.):	 Time base accuracy ±1 count Time base accuracy ± averaging error ± gate error Band A: $\frac{200}{\sqrt{PW-.03}}$ Band B: $\frac{100}{\sqrt{PW-.03}}$ Band A: $\frac{60}{\sqrt{PW-.03}}$ Band B: $\frac{30}{\sqrt{PW-.03}}$ Band A: $\pm \frac{100\ kHz}{PW-.03}$ Band B: $\pm \frac{40\ kHz}{PW-.03}$ PW = pulse width in μs.
Time Base:	Standard / Option P1
Oscillator Type:	Room Temperature Crystal / Temperature Compensated Crystal (TCXO)
Crystal frequency:	10 MHz
Stability: Aging rate: Temperature: (0-50°C)	 $< \lvert 3 \times 10^{-7} \rvert$ /mon. $< \lvert 3 \times 10^{-5} \rvert$ / $< \lvert 2 \times 10^{-6} \rvert$
Line voltage:	±10% change produces frequency shift $< \lvert 1 \times 10^{-7} \rvert$
Warm up time:	None required

Sensitivity: Band A (Opt. P2): Band B:	 300 to 950 MHz -10 dBm peak 925 MHz to 10 GHz -10 dBm peak 10 GHz to 18 GHz -5 dBm peak
FM Tolerance Band B (minimum):	CW: 40 MHz p-p deviation for mod. rates DC-10 MHz. PULSE (w/o Input Inhibit): 20 MHz max. freq. shift across pulse. FREQUENCY PROFILE (using Input Inhibit): 20 MHz max. freq. shift during input inhibit pulse.
Maximum Input Level (peak): Band A: 300 to 950 MHz (Opt. P2) Band B: 925 MHz to 18 GHz	Operating / Burnout Level +10 dBm / +27 dBm +10 dBm / +30 dBm
Input Impedance: Connector:	Band A (Opt. P2): 50 Ω nom., BNC / Band B: 50 Ω nom., Type N precision
Measurement Speed (Band B Only): Acquisition Time: PRF >100 Hz: PRF <100 Hz: Reading Time Band B (sec): 100 μs Gate: 1 ms Gate:	 100 msec + 50 msec/GHz 100 msec + $\frac{5}{PRF}$ sec/GHz Band A: $\frac{400}{(PW)(PRF)}$ Band B: $\frac{100}{(PW)(PRF)}$ Band A: $\frac{4000}{(PW)(PRF)}$ Band B: $\frac{1000}{(PW)(PRF)}$ PW = pulse width (μsec) PRF = pulse repetition frequency (Hz)
Display:	7 digit LED with fixed decimal point. Leading zero suppression.
Resolution:	10 kHz, 100 kHz, 1 MHz
Power:	100/120/220/240 VAC ±10%, 50-60 Hz, 100 watts nominal.

GENERAL SPECS. CONT'D.

Operating Temperature:	0 to 50°C
Weight:	Net 30 lbs. Shipping 35 lbs.
Dimensions:	3.5" high and 16.75" wide and 19" deep
Accessories Furnished:	8 foot power cord and instruction manual
Accessories Available:	Model 400 Delay Generator. Carrying Case. P/N 5700001 Rack Mtg. Kit. P/N 2010008

TABLE 1-1. SPECIFICATIONS - 451 MICROWAVE PULSE COUNTER

FRONT PANEL:

Controls:	
Sample Rate/Hold:	Varies display reading time from 0.1 sec/reading to 10 sec/reading. "Hold" displays last reading.
Test-200 MHz:	Displays 200 MHz internal test frequency.
Display Test:	Tests all LED numeral segments.
Resolution:	(1 MHz, 100 kHz, 10 kHz): Sets display resolution.
1 ms Gate:	Selects 1 ms gate.
Band Select (A or B):	Switch selects either Band A (Opt. P2) or Band B input.
Auto/Manual (Band B):	
Auto Mode:	Band B searches upward for input signal beginning 100 MHz above preset number.
Manual Mode:	Inhibits search. Signal must lie between 100 MHz and 325 MHz above preset number.
Thumbwheel Switch (Band B):	
Auto Mode:	Sets start point of frequency sweep (100 MHz above preset number.)
Manual Mode:	Sets operating frequency range (100 MHz to 325 MHz above preset number.)
Indicators:	
Level:	Indicates sufficient input level.
Lock:	Indicates signal acquired.
Gate:	Indicates measurement in process.
Remote:	Indicates Remote Programming (Option P4 or P5) active.
Reduce Signal (Band B):	Indicates excess signal level.
Connectors:	
Band A input:	Type BNC female - 300 to 950 MHz (Option P2)
Band B input:	Type N precision female - 925 MHz to 18 GHz

REAR PANEL:

Controls:	
Power input:	Power module containing AC connector, fuse, and voltage control for 100, 120, 220, or 240 VAC.
Storage (On/Off):	Normally on. In off position, display updates continuously during measurement cycle.
Min. PRF = (50 Hz/0):	Normally in 50 Hz position. In 0 position, allows measurements of very low PRF signal.
Connectors:	
10 MHz reference output:	1 V peak-to-peak min. into 50 Ω
Gate Output:	-0.5v min. into 50 Ω corresponding to counter gate.
Signal Threshold Output:	-0.5v min. into 50 Ω corresponding to signal exceeding threshold.
Inhibit Input:	ECL high (-0.9v) inhibits. ECL low (-1.7v) enables. From 50 Ω source, 0 volts will inhibit, -1v will enable. Input impedance: 50 Ω to -2 volts.

MODEL / OPTIONS:

Model 451	Microwave Pulse Counter
P1:	TCXO - temperature compensated crystal oscillator
P2:	Band A: 300 - 950 MHz
P3:	Rear panel inputs: Band A and B
P4:	BCD output/remote programming Remote programming: provides rear panel programming of all front panel controls except SAMPLE RATE. Requires ground contact closure; one control line per function (T^2L and DTL compatible). Digital output: 7 data digits in parallel form. 1-2-4-8 "1" state positive.
P5	GPIB: System interface per IEEE STD 488-1975.

TABLE 1-1 (Continued). SPECIFICATIONS - 451 MICROWAVE PULSE COUNTER

SECTION 2

INSTALLATION

2-1. UNPACKING

2-2. The EIP Model 451 Microwave Pulse Counter arrives ready for operation. Carefully inspect the shipping carton before opening for any evidence of visible or concealed damage. If any seems apparent, ask that the shipper's agent be present when the counter is unpacked.

2-3. Remove the packing carton and supports, being careful not to scar or damage the counter. Make a complete visual inspection of the counter, checking for any damage or missing components. Check that all switches and controls operate mechanically. Report any damage to EIP immediately.

2-4. INSTALLATION

2-5. There are no special installation instructions for the 451 Pulse Counter. The unit is a self-contained bench or rack mounted instrument, which only requires connection to a standard, single-phase, 100/120 or 220/240 volt, 50-60 Hz power line for operation. CAUTION: Check current rating of counter fuse and voltage range PC board in power module (on rear panel of counter) before applying power to the counter. Module PC board should show the correct nominal line voltage when installed in the module.

2-6. INCOMING OPERATIONAL CHECK

2-7. The following procedure outlines an operational check of the counter which may be conducted without special tools, signal generators, or test equipment. The internal Time Base Clock is used as the input signal to the Direct Counter, therefore it cannot check the operation of the Band A Prescaler or the Band B Converter.

a. Turn counter **POWER** switch off. Check fuse rating and card in power module (see paragraph 2-5).

b. Connect counter power cord to the voltage source specified in paragraph 2-5. The ground terminal on the power cord plug should connect to a reliable earth ground.

c. Press **POWER** switch (on front panel) to turn counter on. The counter display should light, and the internal cooling fan should operate.

d. Partially depress either of the two **RESOLUTION** switches and release it, so neither switch remains in the depressed position. All digits in the display should indicate "0" (zero).

e. Depress the front panel **200 MHz TEST** switch. The display should indicate "200.00" (200 MHz). Note that the two leading zeros are blanked (not lit).

f. Blank the 10 kHz digit by pressing the right hand **RESOLUTION** switch.

g. Depress the **200 MHz TEST** button again. The display should indicate "200.0".

h. Test both **RESOLUTION** switches. Note that the digit immediately above the switch, and any digit to the right will be blanked.

i. Unblank all display digits (see "d" above).

j. With no input signal, the entire display should show all zeros in both positions of the **BAND** switch.

k. Depress the **DISPLAY TEST** switch. All display digits should show "8" (all segments of each digit lighted).

l. This completes the counter operational check.

SECTION 3

OPERATION

WARNING

DO NOT APPLY A SIGNAL EXCEEDING THE MAXIMUM INPUT SPECIFICATION TO ANY INPUT. EXTENSIVE DAMAGE NOT COVERED BY THE WARRANTY WILL OCCUR, EVEN IF THE COUNTER IS TURNED OFF, OR APPEARS TO BE INOPERATIVE.

3-1. INTRODUCTION

3-2. The Model 451 Microwave Pulse Counter has three principle modes of operation: automatic, manual, and externally enabled. This section will describe each of these modes, and will provide information on timing considerations and instrument accuracy.

3-3. CONTROLS, INDICATORS AND CONNECTORS

3-4. Front panel controls, indicators and connectors are shown in Figure 3-1 and described in Table 3-1. Rear panel controls and connectors are shown in Figure 3-2 and described in Table 3-2.

3-5. NUMERICAL DISPLAY BRIGHTNESS ADJUSTMENT

3-6. Apparent brightness of the light-emitting-diode (LED) numerical display may be varied by adjustment of potentiometer A102R35. (R35 is located near the top front of PC Board A102, and is accessible by removing the top cover of the counter.) Adjust R35 clockwise to increase display brightness, or counter-clockwise to decrease the brightness.

3-7. OPERATION IN THE AUTOMATIC MODE

3-8. In this operational mode, either CW or pulse signals can be measured. Connect the input frequency to the appropriate input connector: **Band B** for frequencies between 925 MHz - 18 GHz, or **Band A** (Option P2) for frequencies between 300 MHz - 950 MHz. If the input signal level is sufficient for counting, the **LEVEL** indicator will light. If the proper band and input have been selected, the **LOCK** indicator will light. In Band B, if the input signal level is too high, the **REDUCE SIGNAL** indicator will light. Measurements will be made at a rate determined by the **SAMPLE RATE** control.

3-9. In Band B, acquisition speed may be improved by presetting the start frequency via the thumbwheel switch. The minimum frequency which can be acquired will then be 100 MHz above the switch setting.

CAUTION: An erroneous reading may result if an applied signal is less than 100 MHz above the switch setting.

3-10. OPERATION IN THE MANUAL MODE

3-11. Manual mode operation applies to Band B only, and is achieved by setting the **MANUAL SELECT/AUTO SWEEP** switch to the **MANUAL SELECT** position, and the thumbwheel switch to the proper frequency. In this mode, the operating frequency range is from 100 MHz to 325 MHz above the switch setting. Since no sweep is required, the acquisition time in this mode is virtually eliminated.

CAUTION: Application of signals which lie between 100 - 325 MHz below the switch setting may result in erroneous readings.

3-12. EXTERNALLY ENABLED OPERATION

3-13. The use of the rear panel **INPUT INHIBIT** makes possible a class of measurements known as *dynamic frequency measurements* — measurements made at a specified point in time on a signal whose frequency is some repetitive function of time. When a high level is applied, the 451 is inhibited from making a measurement. Thus a signal at the **INPUT INHIBIT** can be used as an enable signal to make a measurement at a desired time. The width of the enable signal determines the duration of the measurement — typically 40 nanoseconds less than the applied pulse.

3-14. INPUT INHIBIT REQUIREMENTS

3-15. The **INPUT INHIBIT** on the 451 is designed to be compatible with either a 50 ohm impedance pulse generator, or emitter-coupled-logic (ECL) devices. An internal termination of 50 ohms returned to -2 volts makes this dual compatibility possible. An ECL high level signal (-0.8 to -1.1 V) will inhibit measurement, while an ECL low level signal (-1.5 to -2.0 V) will enable measurement. ECL devices are designed to drive 50 ohm lines without reflections when the lines are terminated with 50 ohms returned to -2 V. The direct compatibility with a 50 ohm pulse generator results from the fact that zero volts from a 50 ohm source will produce -1 V at the **INPUT INHIBIT** (inhibiting the 451), while a -1 V signal into 50 ohms will produce 1.5 V at the **INPUT INHIBIT** thus enabling the 451.

3-16. PULSE PROFILE MEASUREMENTS

3-17. Automatic pulse measurements can determine the average frequency of a pulse. In some cases however, additional information may be necessary. For example, a pulsed magnetron may exhibit substantial frequency shift

(Continued on Page 3-4)

FIGURE 3-1. FRONT VIEW - 451 MICROWAVE PULSE COUNTER

TABLE 3-1. FRONT PANEL CONTROLS, INDICATORS AND CONNECTORS

POWER On/Off Switch

Turns counter power on and off.

SAMPLE RATE/HOLD Control

Continuously variable control for one-tenth to ten seconds per reading. (Required Gate time is added to sample time.) HOLD position retains reading until manually reset.

200 MHz TEST Switch

Provides check of internal counter circuits. Display should indicate "200.00 MHz.

DISPLAY TEST Switch

Displays "88 888.88" to test all LED segments.

RESOLUTION (100 µs GATE) Switches

Provide blanking of either one or two least significant digits for resolution of 10 kHz, 100 kHz, or 1 MHz, with 100 microsecond gate time.

1 ms GATE Switch

Provides 10 kHz resolution with 1 millisecond gate time for reduced pulse averaging error.

RESET Switch

Manually overrides the SAMPLE RATE/HOLD control, resets display to zero, and initiates a new reading.

BAND Select Switches

Select desired operating band — either BAND A (Option P2 - 300 MHz to 950 MHz), or BAND B (900 MHz to 18 GHz).

BAND A Connector

BNC female connector for Band A input (Option P2).

Visual Display

The 7-digit LED (light-emitting-diode) display provides a direct numerical readout of the input frequency. The display is sectionalized into GHz and MHz ranges.

LEVEL Indicator

When lit, indicates that input signal is of sufficient level for counting. Blinking light indicates that PRF (pulse repetition frequency) is too low.

LOCK Indicator

When lit, indicates that input signal has been acquired.

GATE Indicator

Indicates that counter is in measurement portion of its cycle.

REMOTE Indicator

Used with Option P4 (BCD/Remote Programming). When lit, indicates that Remote Enable has been activated, and that all front panel controls except SAMPLE RATE are disabled.

MANUAL SELECT/AUTO SWEEP Switch

Selects manual or automatic operation for Band B.

PRESET/START FREQUENCY Thumbwheel Switch

In the MANUAL mode, the switch sets the operating frequency range. The signal must lie between 100 MHz to 350 MHz above switch setting. In the AUTOMATIC mode, the switch sets the start of the search range. Input frequency must be at least 100 MHz above switch setting.

REDUCE SIGNAL Indicator

Indicates excessive signal input to Band B. WARNING: Signals in excess of rated specifications may cause extensive damage NOT covered by the warranty.

BAND B Connector

Type N precision connector for Band B operation.

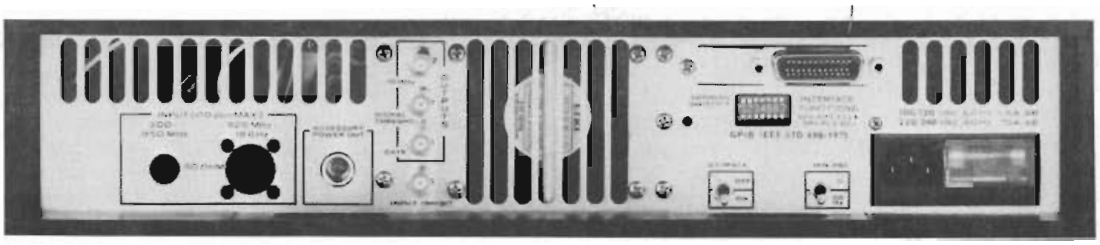


FIGURE 3-2. REAR VIEW - 451 MICROWAVE PULSE COUNTER

TABLE 3-2. REAR PANEL CONTROLS AND CONNECTORS

Rear Panel Inputs

(Option P3) Allows modification of counter for rear panel inputs.

ACCESSORY POWER OUT Connector

Provides power for 451 Pulse Counter accessories.

10 MHz OUTPUT Connector

Output of internal 10 MHz clock, 1 V p-p min into 50 ohms.

SIGNAL THRESHOLD OUTPUT Connector

Pulse output representing signal threshold level of input pulse. Typically occurs 20 nanoseconds after input pulse, and is used for frequency profile measurements.

GATE OUTPUT Connector

Provides Gate pulse representing actual time at which measurement is being made. Used in frequency profile measurement.

INPUT INHIBIT Connector

External pulse input for frequency profile measurements.

Remote Input/Output Connector

(Option P4) Connector for BCD/Remote Programming.

GPIB Input/Output Connector

(Option P5) For connection to General Purpose Interface Bus (IEEE STD 488-1975). Refer to separate Instruction Manual for EIP Model 451 Option P5.

STORAGE Switch

Normally ON. In the OFF position, display updates continuously during measurement cycle.

MIN PRF Switch

Normally in 50 Hz position. In 0 position, allows measurement of very low PRF signal. NOTE: Reading will not automatically reset when signal is removed.

AC Power Module

Contains AC power line receptacle, fuse, and PC board for voltage selection.

near the leading and trailing edges of the pulse, or a pulsed Gunn diode oscillator may exhibit frequency shift during a pulse due to peak power thermal effects. Measurements of these characteristics are easily made with only the 451 and a delaying pulse generator (see Figure 3-3). The SIGNAL THRESHOLD output of the 451 is used to trigger the pulse generator. The generator's output pulse is used as an enable input to the 451. As the pulse delay is varied, the measurement window can be "walked" through the pulse. A plot of frequency-versus-delay gives the frequency-versus-time profile of the pulse directly as shown in Figure 3-4. The width of the measurement window is determined by the width of the pulse generator output. Measurement windows of 50 nanoseconds or less can be used, although wider windows yield higher accuracy.

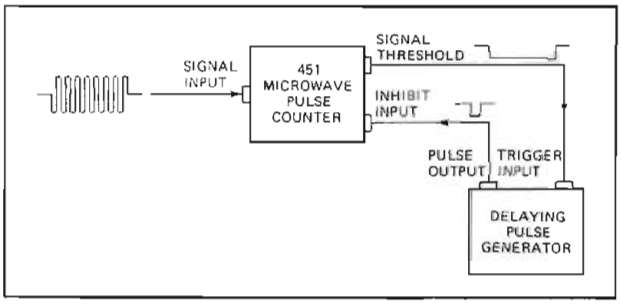


FIGURE 3-3.
PULSE PROFILE MEASUREMENT TEST SET-UP

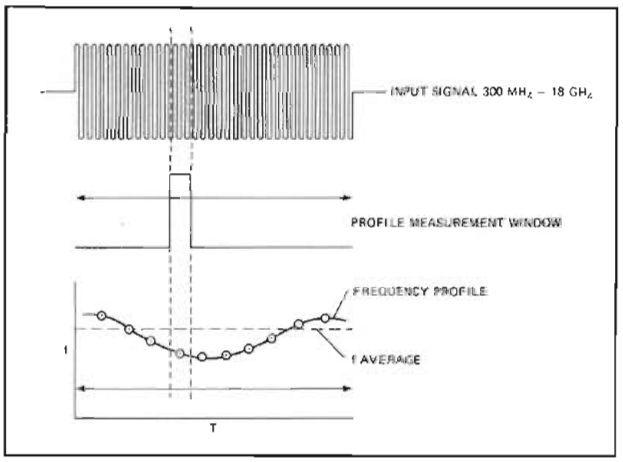


FIGURE 3-4. PULSE PROFILE MEASUREMENT

3-18. DYNAMIC CHARACTERISTICS OF TIME VARYING SIGNALS

3-19. Many complex signals are not pulses at all but simply continuous signals whose frequency varies repetitively with time. One example is the measurement of the response of a device such as a voltage controlled oscillator (VCO). A square wave applied to the tuning voltage will produce a response curve of frequency-versus-time allowing measurement of various settling times such as post-tuning drift. Another possible application would be the measurement of linearity and amplitude for frequency modulated radar altimeter signals. Figure 3-5 shows a test set-up designed to make measurements on time varying signals. It is similar to the pulse profile test set-up, except that in this case since there is always a signal present, a trigger must be obtained from the modulating source. This will trigger the pulse generator which controls the measurement.

3-20. MULTIPLE PULSE SIGNAL MEASUREMENTS

3-21. Another type of measurement is that of a repetitive sequence of pulses differing in frequency. In this case, it is desirable to measure the frequency of each pulse in the sequence separately. The same test set-up as shown in Figure 3-5 is required, with the trigger pulse synchronous with the sequence. In this measurement, the INPUT INHIBIT is used simply to discriminate between pulses. The enabling pulse can be slightly wider than the pulse to be measured. The 451 will automatically restrict the measurement window entirely within the pulse. By shifting the delay time of the enabling pulse, each input pulse of the sequence can be separately measured.

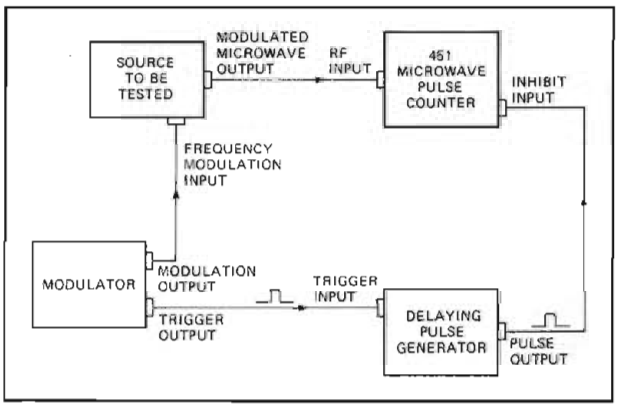


FIGURE 3-5.
TIME VARYING SIGNAL MEASUREMENT TEST SET-UP

3-22. TIMING CONSIDERATIONS

3-23. Under most circumstances, internal timing within the 451 would be of no concern to the user. However, in applications where a few nanoseconds are significant, some details of internal operation are important. These involve two areas: (a) measurement window width, and (b) internal timing delays.

(a) Measurement Window Width

The measurement window is the period during which the GATE is actually open to enable the counting of a signal. This GATE width will typically be 30 nanoseconds narrower than the pulse applied to the INPUT

INHIBIT. The width of the GATE is always an integral number of clock periods (5 nanoseconds). For applications where the measurement window needs to be known to an accuracy better than 20 nanoseconds, it is recommended that the GATE output on the 451 rear panel be observed directly on a high speed oscilloscope. The desired GATE width may then be set by varying the INPUT INHIBIT pulse width. For accurate pulse representation, the oscilloscope input should be terminated in a 50 ohm load.

(b) Internal Timing Delays

When it is necessary to measure the signal frequency at a precise point in time, the internal delays of the measuring instrument can be significant. In the 451, the total delay between the time a signal is applied to an input connector, and the time it is available to be counted, is nominally 60 nanoseconds. The SIGNAL THRESHOLD output on the rear panel of the 451 typically occurs 20 nanoseconds after the signal is applied. The GATE signal at the rear panel occurs at the measurement time with virtually no delay. In other words, when absolute time positioning of a signal is required, it is necessary to consider that the GATE signal, which represents the measurement period, is actually making a measurement of the signal which appeared at the input connector 60 nanoseconds earlier. If the SIGNAL THRESHOLD output is used as an indication of input signal, then it occurs 40 nanoseconds prior to measurement. Figure 3-6 shows the relative timing of these signals for a pulsed input signal. Timing however, is not a function of input signal characteristics.

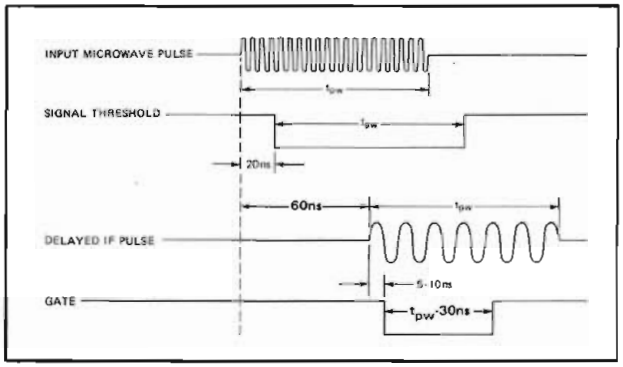


FIGURE 3-6. INTERNAL TIMING DELAYS

3-24. ACCURACY

3-25. In a CW frequency counter, measurement accuracy is generally specified as "time base accuracy ± 1 count". This means that the frequency measurement is in error by the same percentage as the time base reference oscillator. The maximum error in the time base is the sum of various possible errors, such as aging rate, temperature, etc.

3-26. The second type of error: ± 1 count, is derived from the relative timing of gate and signal. Simply stated, if an event occurs every 400 ms (F = 2.5 Hz), a counter could measure either 2 or 3 events in a one second interval.

3-27. There is a third possible source of error in a CW counter: gate error. A gate is supposed to represent a precise number of reference oscillator cycles. Due primarily to differences in the rise and fall times of various circuits, the actual gate will usually be a fixed amount wider or narrower than desired. If this error is less than one period of the maximum input frequency, no counter error will occur. Thus a 300 MHz counter needs a gate accurate to about 3 nanoseconds.

3-28. Each of these three sources of error can contribute to the overall error in pulse frequency measurements. In fact for narrow pulses, the second and third sources of error which are usually ignored in a CW counter, become the dominate sources of error in a pulse counter.

3-29. Time Base Errors

3-30. A frequency error in the time base reference oscillator, results in a proportional frequency measurement error. Two main sources of time base error are: aging rate, and temperature. Aging rates of $< |3 \times 10^{-7}|$/month, and temperature stability of $< |3 \times 10^{-5}|$ over the range of 0 to +50° C, are standard on the 451. An optional temperature compensated crystal oscillator (TCXO) reduces temperature instability to $< |2 \times 10^{-6}|$. By calibration against a frequency standard, this error can be made less than one one count, and thus becomes insignificant.

3-31. Averaging Error

3-32. In order to obtain high resolution, the frequency of a number of measurements is averaged. Each individual measurement has a ± 1 count uncertainty as previously noted. If N measurements are made, then an uncertainty of ± N counts is possible, but very unlikely. The resultant averaged measurement will follow the rules of statistics, in that successive measurements will vary randomly to a certain degree. In fact, most of the readings (63%) will fall between $\pm \sqrt{N}$ counts — this is called the RMS averaging error. N is the number of gates required to accumulate 100 ms (or 1 µs) of gate time. The gate is typically 30 ns narrower than the input pulse, so the RMS averaging error is:

$$\text{Averaging Error (RMS)} = \frac{100 \text{ (or 30) kHz*}}{\sqrt{PW - .03}}$$

PW = Pulse width in ms. * 30 kHz with 1 ms gate, 200 (or 60) kHz for Band A. NOTE: Since Band A gate times are expanded by 4, $\sqrt{N}$ increases by 2.

3-33. Gate Error

3-34. When narrow pulses are counted, the gate is opened many times in order to obtain a high resolution measurement. Each time the gate opens and closes, there will be a small but finite error. The total error is proportional to the number of times the gate is cycled during a measurement, and is thus inversely proportional to the gate width. This error is also related to both temperature and

input frequency. In the 451, the worst case error including all variables, is specified as:

$$\text{Max Gate Error} = \frac{40 \text{ kHz}}{PW - .03}$$

where PW = pulse width in microseconds.

Unlike averaging error which is random, gate error is systematic, and is not reduced by frequency averaging.

3-35. TECHNIQUES FOR IMPROVING ACCURACY

3-36. In most cases, specified accuracy of the 451 will be more than sufficient to meet measurement requirements. If greater accuracy is required, all three sources of error can be minimized by a combination of error calibration and long term averaging. It is recommended that if very high accuracy is required, the counter include Options P1 (TCXO) and P4 (BCD Output/Remote Programming).

3-37. Time Base Calibration

3-38. A frequency error in the time base oscillator results in the same percentage error in the frequency reading for either CW or pulsed signals. By directly measuring the 10 MHz time base frequency at the 10 MHz OUTPUT connector using a standard of known accuracy, this error can be determined and corrected. As an example, suppose the measured time base output is 10.0001 MHz. The time base is thus 1×10^{-6} high in frequency, and all readings will be 1×10^{-6} low in frequency — a reading at 10 GHz will be 10 kHz low. Instead of correcting the *reading* for this error, a better technique is to set the time base oscillator precisely on frequency. The advantage of a 451 equipped with a TCXO is improved settability and temperature stability.

3-39. Long Term Averaging

3-40. Averaging error, as noted previously, is simply the result of a random statistical process. As in all such processes, taking a larger number of samples reduces the averaging error. On 451's equipped with BCD Output Option P4, a test set-up as shown in Figure 3-7 allows the random averaging error to be virtually eliminated. The DAC takes the three least-significant-digits and produces an analog voltage which is plotted on a strip chart recorder. The average value of the output can be easily obtained from the strip chart.

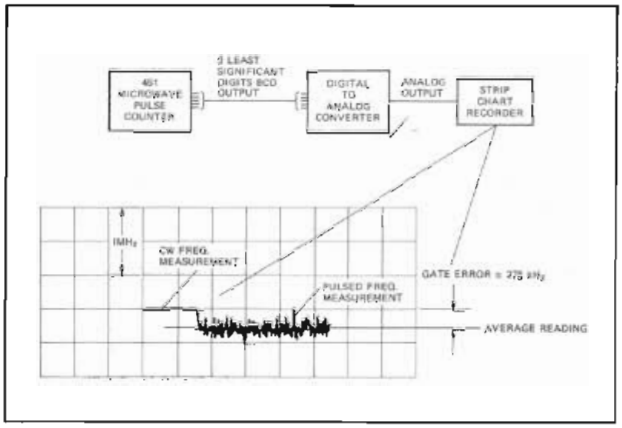


FIGURE 3-7.
CALIBRATION TEST SET-UP (AVERAGING/GATE ERROR)

3-41. Gate Error

3-42. Gate error at any given frequency and pulse width can be virtually eliminated — this is accomplished by simulating a pulsed input and determining the gate error. This calibration factor can then be added to, or subtracted from, the indicated measurement to obtain the correct frequency. First, determine the gate error using a CW source at approximately the same frequency (within 25 MHz) as the indicated measurement. A pulsed input is then simulated by applying an ENABLE signal — of the same width as the pulse to be measured — to the INPUT INHIBIT connector. Gate error is the difference in reading between the pulsed and non-pulsed measurement of the same CW signal. This procedure provides the true gate error, and avoids error associated with any possible pulling of the signal source. The DAC and strip chart recorder shown in Figure 3-7 can be used to determine the error to a resolution of a few kHz. The result of a typical strip chart is also shown. It should be noted that gate error can be calibrated out of the system for a given pulse width and frequency. However, this calibration procedure will result in additional error for any other pulse width or frequency.

SECTION 4

GENERAL THEORY OF OPERATION

4-1. GENERAL

4-2. The EIP Model 451 Microwave Pulse Counter automatically measures and displays the frequency of a CW or pulsed signal in the range of 925 MHz to 18 GHz (Band B). An optional Prescaler (Option P2) extends this range downward to 300 MHz (Band A). In addition to fully automatic measurements, it is possible to utilize the 451 with accessory equipment to make dynamic frequency measurements — the frequency of any repetitive signal can thus be measured at any point in time. Measurement windows as narrow as 20 nanoseconds are achievable.

4-3. Measurements in Band B (925 MHz - 18 GHz) are achieved by heterodyning the input signal with a known harmonic of 200 MHz. The resulting difference frequency is then processed by a 350 MHz Direct Counter. The counter gate is enabled by the input itself in a manner such that the gate is open only when a signal is present.

4-4. In the Direct Counter, obtainable resolution is inversely proportional to the measurement time. For example: a 1 microsecond gate time will yield 1 MHz resolution. To achieve 10 kHz resolution, the 451 automatically averages as many input pulses as necessary to obtain a total gate interval of 100 μs (or 1 ms). The required number of pulses is thus a function of the input pulse width. (A more comprehensive discussion of this will be found beginning with paragraph 4-27.)

4-5. In the optional Band A (300 MHz - 950 MHz), the input frequency is divided by four. The divided frequency is then counted in the Direct Counter for a 400 μs (or 4 ms) period to obtain a readout with 10 kHz resolution. As in Band B, gating is controlled by the input signal.

4-6. The system operation of the 451 is best described by separating the instrument into its two main functional blocks: the Microwave Converter, and the Direct Counter.

4-7. Figure 4-1 shows a simplified block diagram of the entire 451. Figure 4-2 shows a more complete block diagram of the Microwave Converter section, while Figure 4-3 diagrams the Direct Counter. Detailed circuit descriptions of all PC boards are given in Section 9.

4-8. MICROWAVE CONVERTER

4-9. The Microwave Converter is a self-contained assembly which performs the function of translating the input microwave frequency downward into the range of 100 to 350 MHz. This translation is accomplished by mixing the incoming signal with a known reference frequency and then amplifying the difference. The input frequency is determined by counting this difference frequency and adding it to the known reference frequency (see Figure 4-2).

4-10. The reference frequency is an integral harmonic of 200 MHz, generated within the YIG Comb Generator (A207). This unit is an integrated assembly containing a harmonic (or comb) generator, and a two-stage YIG filter. The comb generator converts the 200 MHz sine wave input into a train of narrow pulses containing all the harmonics of 200 MHz up to 18 GHz, while the YIG filter selects the desired harmonic. Tuning of the YIG filter is accomplished by varying the current through a pair of coils, which in turn, varies a magnetic field within the structure. (A more comprehensive description of the operation of a YIG-tuned device is given later in this section.)

4-11. The 200 MHz reference is generated within Source/Amplifier A201 by an LC oscillator which is phase-locked to the 10 MHz Time Base Oscillator (A108) within the 451. This reference is amplified to produce up to one watt of output power to drive the comb generator section of A207. A second output at 200 MHz is used to generate the gate and test functions within the Direct Counter.

4-12. The RF input signal to the Converter section first passes through a Limiter/Attenuator (A206). The limiter portion of this module is a passive diode whose main function is to protect the Mixer (A205) against excessive input power. Protection at levels up to one watt peak or average is provided. The attenuator section contains a multistage, matched PIN diode serving two functions: (a) to provide a means of controlling the RF signal level to the Mixer, and (b) to act as a switch which shuts off the input signal during certain portions of Converter operation.

4-13. The Mixer (A205) is another integrated microwave circuit assembly, containing a hybrid coupler, termination, mixer diode, and a DC return. The Mixer produces two output signals on a common line: (a) an IF signal equal in frequency to the difference between the RF signal and the reference signal; (b) a Video signal resulting from rectification of either the RF or reference input.

4-14. The IF and Video signals are separated in the IF Processor (A204). This assembly contains an IF amplifier, video amplifiers, threshold circuits, and LOCK circuitry. The output of the IF amplifier is the signal actually measured by the Direct Counter. It is also used by the LOCK circuitry to determine the correct reference frequency (comb line). The Converter is considered to be locked when a particular comb line mixes with the applied RF signal to produce an IF signal of proper amplitude and frequency.

4-15. The amplified Video output is used to generate three separate signals: two threshold, and one analog output. One signal — SIGNAL THRESHOLD — is used to detect the presence of sufficient RF signal to initiate operation of the Converter and enable the gate of the Direct Counter. The

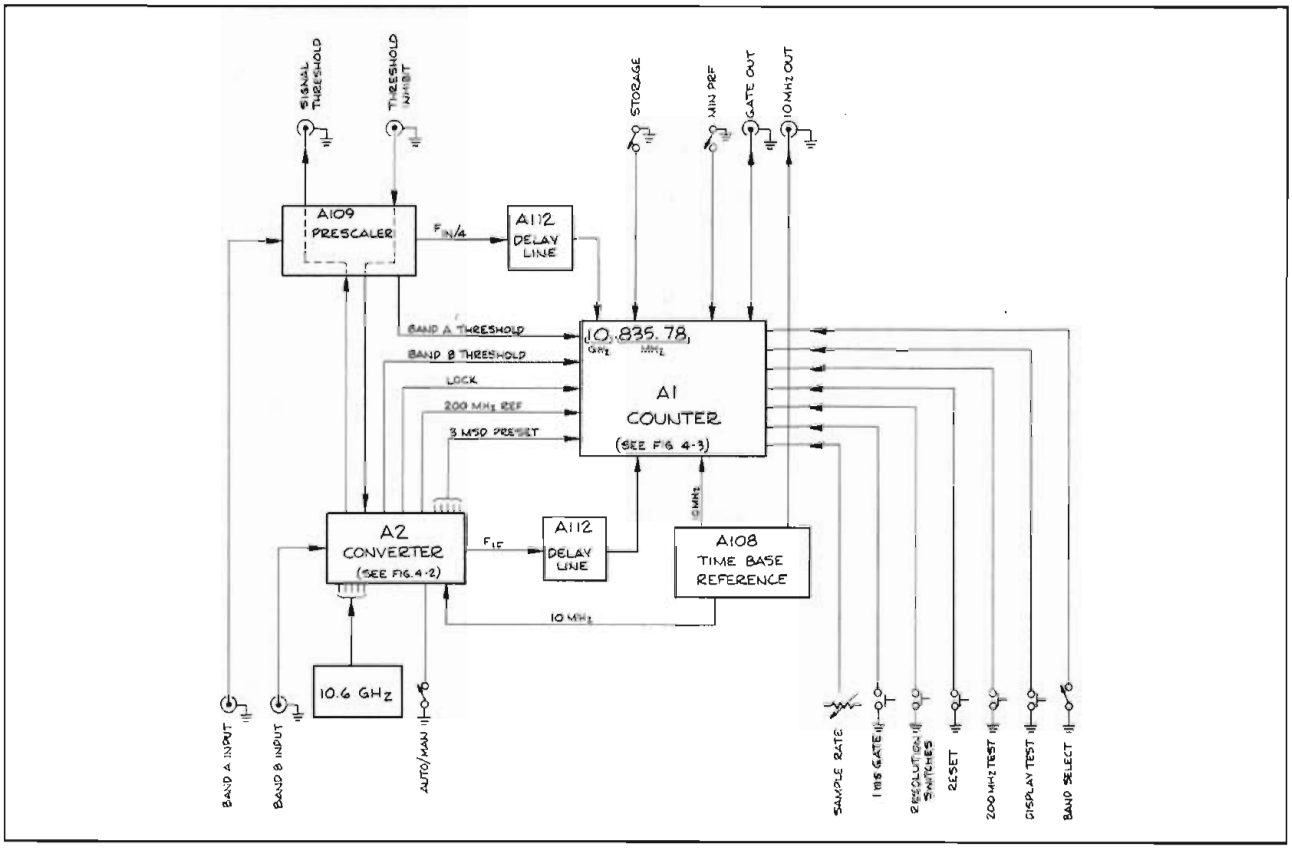


FIGURE 4-1. BLOCK DIAGRAM - 451 MICROWAVE PULSE COUNTER

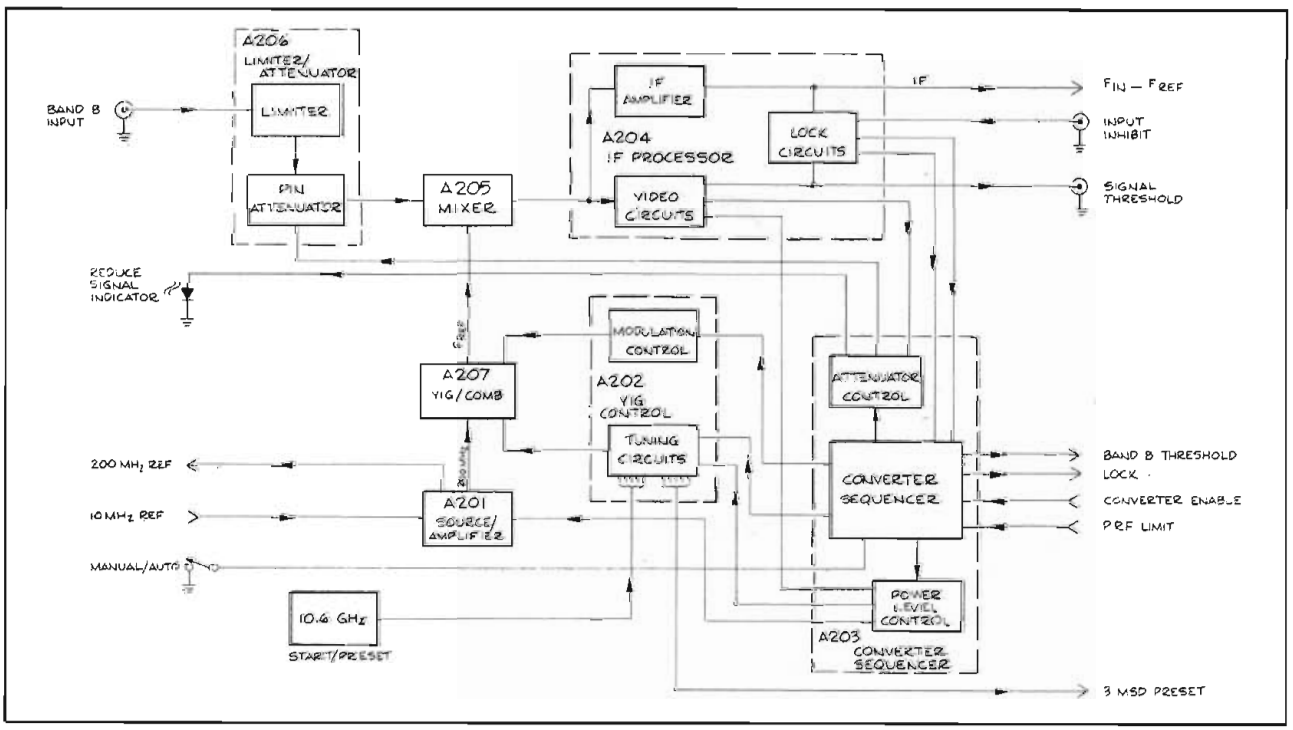


FIGURE 4-2. BLOCK DIAGRAM - 451 PULSE COUNTER - CONVERTER (A2)

second threshold — ATTENUATOR CONTROL — is activated at a level approximately 7 dB above SIGNAL THRESHOLD, and causes the attenuator to reduce the input signal level. The third signal is an analog output corresponding to the amplitude of the reference signal, and is used in the process of stepping from one comb line to another.

4-16. YIG Control board A203 contains all the functions necessary to step the YIG filter to the proper comb line. The primary circuits are a YIG Driver to supply the required current, a digital-to-analog converter (DAC) to set the approximate center frequency, and a centering circuit to precisely center the YIG filter passband on a comb line. The centering process involves modulating the YIG center frequency via an auxiliary modulation coil in the YIG structure. The modulation circuitry is also located on the YIG Control PC board.

4-17. The remaining major assembly in the Converter is the Converter Sequencer (A203). This assembly contains the power level control function to set comb line amplitude, the attenuator control function, and the Converter Sequencer — which acts as the major control unit for the entire Converter. (A detailed operational sequence is given in Section 9).

4-18. 350 MHz DIRECT COUNTER

4-19. After an RF signal is translated into the range below 350 MHz, the frequency is determined by the 350 MHz Direct Counter. This is accomplished by accumulating the number of cycles of the signal which occur within a precisely determined time interval. This interval is based on the frequency of the Time Base Oscillator. In the 451, the total time intervals used are 100 microseconds and 1 millisecond. In order to measure narrow pulses to a resolution of 10 kHz, it is necessary to add together the number of cycles counted in each of a large number of pulses, until the required total time interval is obtained.

4-20. The Direct Counter consists of several major functional blocks as shown in Figure 4-3. Input signals are applied to High Frequency board A106, where they are processed into a standardized signal suitable for counting. This signal then passes through the counter gate to the first decade of the counting chain, which accumulates the input count. The output of this decade goes to the Count Chain (A103) which contains the remaining six decades. A103 also includes the storage unit which holds all the digital information of the previous reading.

4-21. Information display is controlled by Count Chain Control (A102), which contains all the required multiplexing circuitry to drive the Display (A110). The logic to suppress leading zeros on the display is also on A102.

4-22. Overall control of the 451 Counter is performed by the Control board (A104). This assembly generates the counter operating sequence, and interfaces with most of the operating controls as well as the Converter and Prescaler.

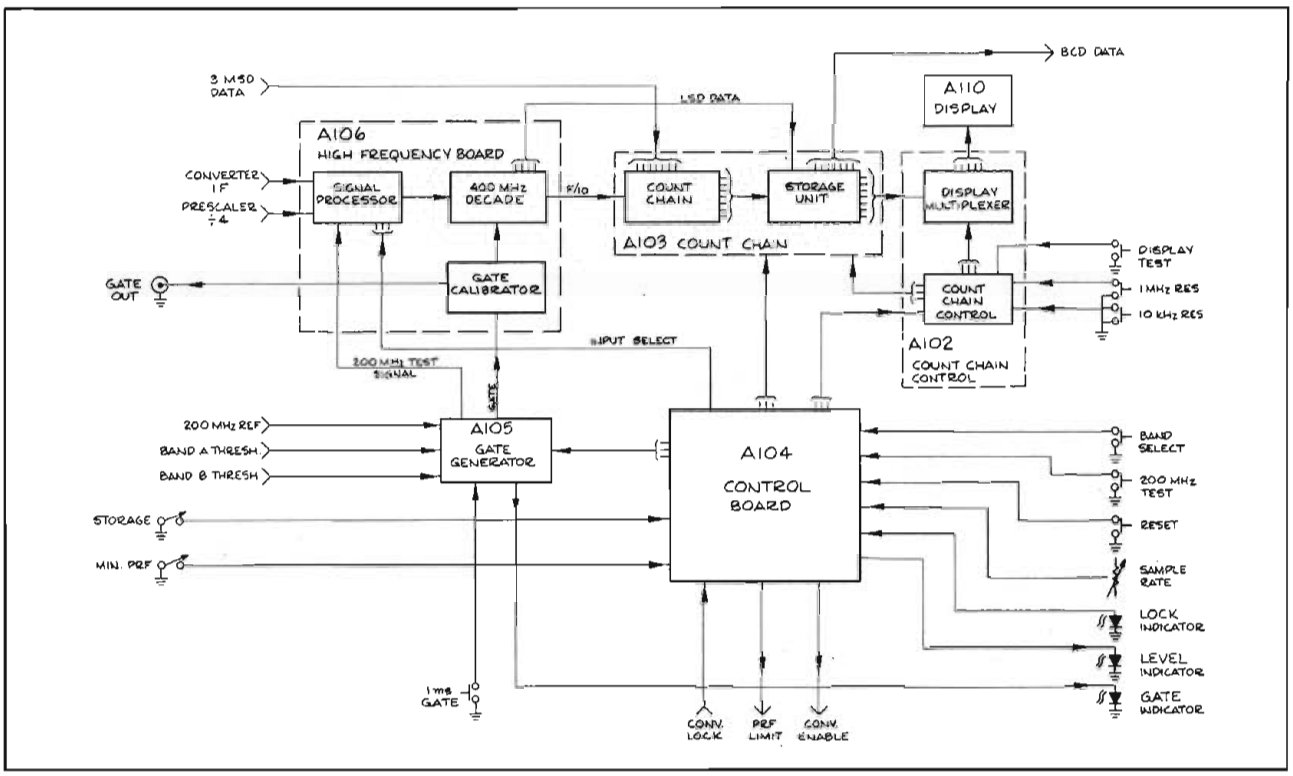


FIGURE 4-3. BLOCK DIAGRAM - 451 PULSE COUNTER - DIRECT COUNTER (A1)

4-23. GATE GENERATOR

4-24. The remaining function of the counter, that of generating a precision gate, is accomplished by the Gate Generator (A105). This function is considerably more difficult for pulsed signals than it is for CW signals, and it is on this function that the overall accuracy of the 451 depends. Two separate operations are performed — the first is to supply a GATE to the High Frequency board which is present only when an input signal is also present. The second is to accumulate the total time during which the GATE is applied, until 100 microseconds (or 1 millisecond) is reached.

4-25. The first operation requires that the GATE begin after the signal is present at A106, and end prior to the end of the signal. This is accomplished by generating a GATE approximately 30 nanoseconds shorter than the RF signal (as determined by the SIGNAL THRESHOLD level). The arrival time at A106 of the IF from the Converter (or Prescaler), is then controlled by a delay line so the GATE will fall entirely within the IF pulse.

4-26. The second operation is accomplished by counting clock pulses whenever the GATE is open, until a total time of 100 μs (or 1 ms) is obtained. This requires that each GATE opening is for an exact integral number of clock pulses. A 200 MHz clock is used for this, causing the GATE width to be increased in 5 ns steps until a total of 20,000 (or 200,000) clock pulses is accumulated.

4-27. ACCURACY

4-28. In the case of a CW measurement, absolute accuracy is determined almost entirely by the Time Base Reference frequency accuracy. In turn, this accuracy is a function of initial calibration and reference stability with time and temperature.

4-29. The remaining inaccuracy is the digital counting error, specified as ± 1 count, and is normally insignificant in CW measurements. It results from the fact that the number of periodic events that occur in a fixed time interval can vary by one, depending upon the phase of the signal.

4-30. When considering pulse measurement accuracy, the digital counting error can become highly significant, especially for narrow pulses. This results from the fact that the error is a random error, which occurs every time the GATE is opened. Since the error is random, it is subject to statistical fluctuations. This averaging error is proportional to $\sqrt{N}$, where N is the number of times the GATE is opened during a measurement. This, in turn, can be related directly to pulse width:

$$\text{Averaging Error (RMS)} = \frac{100\,(\text{or } 30)\text{ kHz}^*}{\sqrt{PW - .03}}$$

PW = Pulse width in microseconds.
* 30 kHz with 1 ms gate, 200 (or 60) kHz in Band A.

Since the averaging error is random, its contribution to overall measurement error can be made arbitrarily small by mathematically averaging multiple readings.

4-31. The second source of error in pulse measurement is GATE error. This error results from a GATE which is not an exact intregral multiple of the clock period. In the measurement of narrow pulses, GATE errors of small fractions of a nanosecond can be significant. Each time the GATE is opened, a fixed error is introduced. As a result, the error is proportional to the number of times the GATE is opened. This is a systematic error and will not average out as will the averaging error. The worst case GATE error, including all effects of frequency and temperature, is given by:

$$\text{GATE Error (max)} = \frac{40\text{ kHz}}{PW - .03}$$

PW = Pulse width in microseconds.

If necessary, GATE error at any particular frequency and pulse width, can be calibrated out of the counter.

AN INTRODUCTION TO YIG FILTERS

Highly polished spheres of single crystal YIG (yttrium-iron-garnet), have a property called ferrimagnetic resonance. Basically, the ferrimagnetic resonance phenomenon can be explained in terms of spinning electrons creating a net magnetic moment in each molecule of a YIG crystal (see Figure A). Viewing the material macroscopically, there is no net effect because the magnetic dipoles associated with each molecule are randomly oriented (see Figure B). The application of an external magnetic biasing field, H_{DC}, causes the magnetic dipoles to be aligned in the direction of the biasing field (see Figure C).

An RF field can be used to create an orthogonal magnetic force. If the frequency of the RF field coincides with the natural precession frequency, there is a strong interaction called ferrimagnetic resonance (Figure D).

Figure E shows the basic elements of a YIG bandpass filter. The filter consists of a YIG sphere at the center of two loops. The two loops are perpendicular to each other and to the dc biasing field, H_{DC}. One loop carries the RF input and the other the RF output. When the RF signal frequency is the same as the natural precession frequency of the YIG, there is strong coupling between the input and output loops. Thus RF can only pass through the YIG filter at resonance. The resonant frequency is a linear function of the magnetic biasing field, H_{DC}. Generally, H_{DC} is provided by locating the YIG spheres between the poles of an electromagnet, and tuned by varying the current to the magnetic coils.

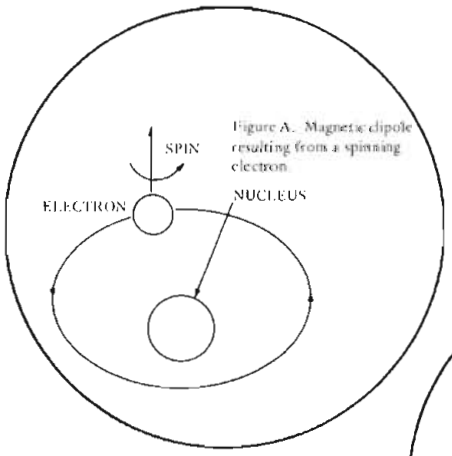


Figure A. Magnetic dipole resulting from a spinning electron.

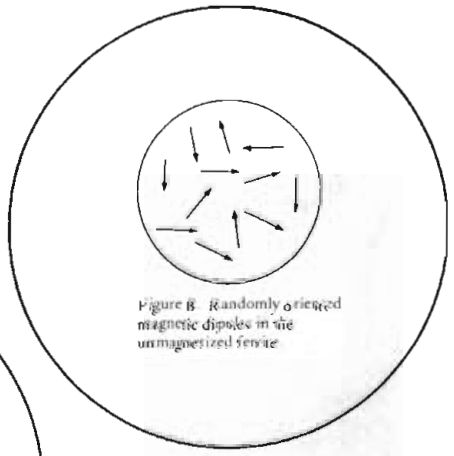


Figure B. Randomly oriented magnetic dipoles in the unmagnetized ferrite.

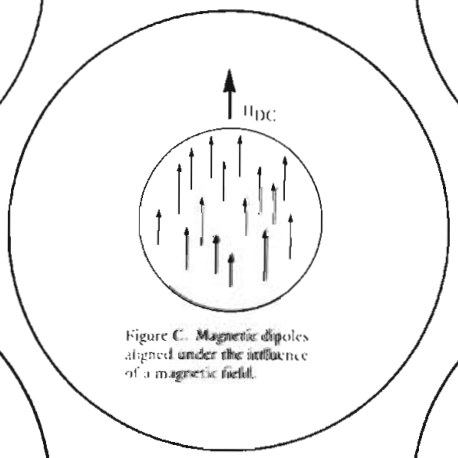


Figure C. Magnetic dipoles aligned under the influence of a magnetic field.

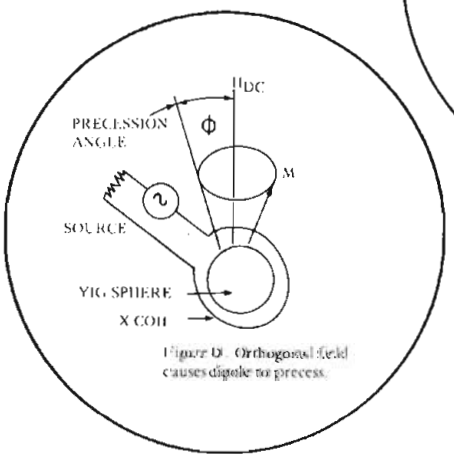


Figure D. Orthogonal field causes dipole to precess.

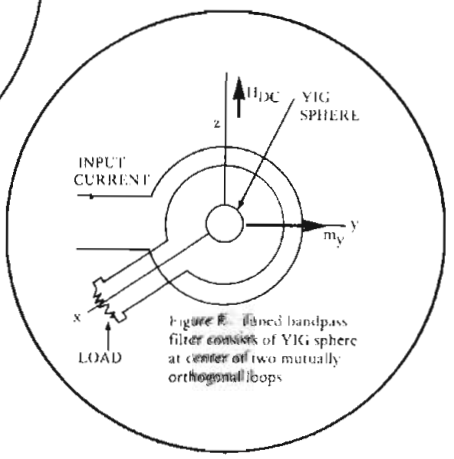


Figure E. Tuned bandpass filter consists of YIG sphere at center of two mutually orthogonal loops.

SECTION 5

MAINTENANCE & SERVICE

5-1. GENERAL

5-2. This section provides instructions, procedures, and information necessary to maintain, troubleshoot, and repair the EIP 451 Microwave Pulse Counter.

5-3. FUSE REPLACEMENT

5-4. The counter uses one fuse, located in the **POWER INPUT** module on the rear panel. For proper operation, use only the fuse specified — do not increase fuse rating or change fuse type. Power module PC board should display the correct nominal line voltage when installed in the module. TO CHANGE TO ANOTHER LINE VOLTAGE:

a. Slide open power module cover and rotate **FUSE PULL** to the left.

b. Select operating voltage by orienting PC board so nominal supply line voltage appears on the top left side of the PC board. Push board firmly into module slot. (NOTE: When board is completely inserted, only the selected operating voltage will be visible.)

c. Rotate **FUSE PULL** back into normal position and insert fuse in holder, taking care to select correct fuse value. Close module cover.

d. For 100/120 VAC operation, use a 1.5 A, Slow-Blow, 3AB/MDX type fuse. For 220/240 VAC operation, use a 0.75 A, Slow-Blow, 3AB/MDL type fuse.

5-5. AIR CIRCULATION

5-6. During operation of the counter, the internal fan draws in cooling air through the vents in the rear panel. If these vents are blocked, the temperature inside the enclosure may rise to the point where counter stability is reduced, and component life shortened.

5-7. COUNTER SERVICING

5-8. Recommended Service Procedures:

a. To remove plug-in PC boards: Turn off power to counter. Ease PC board out of its socket by lifting up on board handles. Remove carefully to avoid placing strain on any connecting cables.

b. To unplug flat ribbon cables: Turn off power to counter. Remove PC board as necessary. Use an IC Extractor Tool (EIP P/N: 5000094 or equivalent) to unplug flat ribbon connector.

c. To remove PCB socket locating key: Key must be turned 90° before removal from or re-insertion into socket to avoid contact damage. Use long-nose pliers for removal or insertion.

d. Internal cable and harness routing is shown both in Figure 9-1 and inside the top cover of the counter.

e. Circuit descriptions of PC board and modular assemblies are shown on the same pages (in Section 9) as the related schematic diagram and component layout.

f. Troubleshooting Trees shown later in this section are intended only as a guide, and do not describe every possible failure situation. To speed troubleshooting of a board, replace the board with a known good one.

g. A listing of recommended test equipment for servicing, calibration, and performance testing, is given in Table 5-1. Other equipment may be used provided performance equals or exceeds that listed.

5-9. Servicing Precautions

a. The following assemblies should be replaced instead of being serviced in the field due to the specialized test equipment and procedures required for recalibration: Source/Amplifier (A201), IF Processor (A204).

b. If the following assemblies are repaired either at EIP or in the field, recalibration in the associated counter will be required for proper operation: Gate Generator (A105), High Frequency (A106), YIG Control (A202), Converter Sequencer (A203).

> CAUTION
>
> DO NOT ATTEMPT REPAIR OR DISASSEMBLY OF THE FOLLOWING COMPONENTS: MIXER (A205), PIN LIMITER/ATTENUATOR (A206), YIG COMB GENERATOR (A207), OR TCXO TIME BASE OSCILLATOR (ON A108).

5-10. FACTORY SERVICE

5-11. If the counter is to be returned to EIP for service or repair, BE SURE TO INCLUDE THE FOLLOWING INFORMATION WITH THE SHIPMENT:

a. Name and address of owner.

b. Model and complete serial number of counter.

c. A COMPLETE description of trouble (e.g: under what conditions did trouble occur? What was the signal level? What associated equipment was attached or connected to the counter? Did that equipment fail too?)

d. Name and telephone number of someone familiar with the problem who may be contacted by EIP for any further information if necessary.

e. Shipping address to which counter is to be returned; include any special shipping instructions.

f. Pack the counter for shipment as follows:

(1) Wrap the counter in plastic or heavy kraft paper, and repack in the original shipping container (if still available) using the original packing material.

(2) If the original container and packing material are no longer available, use a heavy (275 lb. test) double-walled carton, with approximately 4" of suitable packing material between the inner and outer walls, with additional packing material as required between the counter and the inner carton. Seal with strong filamentary tape or strapping.

(3) Mark shipping container to indicate that it contains fragile electronic instruments. Ship to EIP at address shown on title page of this manual.

5-12. TROUBLESHOOTING

5-13. MALFUNCTION AT TURN ON

5-14. If the counter fails to turn on (no display, no fan, etc.), make the following checks:

a. Power module PC board correctly inserted and fuse good (see paragraph 5-4).

b. Power cord plugged into counter and into active AC power source.

c. POWER switch at "on" position (button depressed and green indicator showing).

d. PC boards and connectors are properly engaged.

e. Power supply voltages correct (measure at A100J3); refer to paragraph 6-8 for acceptable tolerances.

5-15. FAILURE TO INDICATE ALL ZEROS

5-16. If counter turns on, but fails to indicate all zeros with no applied signal, CHECK THAT:

a. No RESOLUTION switches are depressed.

b. Rear panel MIN PRF switch is in 50 Hz position.

c. PC boards and connectors are properly engaged.

d. Power supply voltages correct.

e. Perform Visual Display Test by pressing DISPLAY TEST switch on front panel. Display should show the numeral "8" in all decade positions.

f. If counter fails the Visual Display Test refer to Troubleshooting Tree Figure 5-4. If counter displays all eights but a digit is missing, refer to Figure 5-5. If the display does not show all zeros when it should, refer to Figure 5-6.

5-17. MALFUNCTION IN SELF TEST

5-18. If counter turns on, but fails to indicate a reading of 200.00 (200 MHz) in the TEST mode, CHECK THAT:

a. Counter indicates all zeros with no applied signal.

b. PC boards and connectors are properly engaged.

c. Power supply voltages correct.

d. Counter passes Visual Display Test (para. 5-16).

e. Refer to Figure 5-7.

5-19. MALFUNCTION IN BAND A (OPTION P2) (300 MHz to 950 MHz)

5-20. If counter fails to read frequency correctly, CHECK THAT:

a. BAND SELECT switch is in the Band A position.

b. A signal of the proper level and frequency range is applied to the Band A input connector.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Refer to Figure 5-8.

5-21. MALFUNCTION IN BAND B (925 MHz to 18 GHz)

5-22. If counter fails to read frequency correctly, CHECK THAT:

a. BAND SELECT switch is in the Band B position.

b. A signal of the proper level and frequency range is applied to the Band B input connector.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. YIG Control (A202) and Converter Sequencer (A203) PC board and co-ax connectors are properly engaged.

g. Refer to Figure 5-9.

5-23. MODULE FAILURE VERIFICATION

5-24. Source/Amplifier (A201) Power Output Check:

a. Turn off counter power. Remove cable from A201J2.

b. Connect a co-ax cable to A201J2 which is connected to a 30 dB, 1 watt attenuator. Output of the attenuator should be fed to a broadband calibrated detector. CAUTION: 1 watt at 200 MHz can appear at A201J2.

c. Turn on counter. Set counter to Band B.

d. Apply a +5 dBm, 1 - 18 GHz signal to the Band B input connector.

e. Check that Source/Amplifier (A201) has correct power supply voltages, 10 MHz Reference, and Power Reference inputs.

f. Connect dual-trace scope Channel A to A201FL1 (2 V/div), and Channel B to detector output.

g. Set Channel B sensitivity for full scale deflection at 0 dBm into detector (1 W at A201J2).

h. Channels A and B should have similar waveforms, with maximum detector output approximating 1 watt at A201J2 (see Figure 5-1).

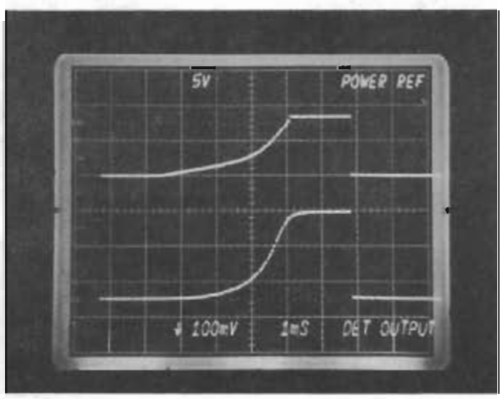


FIGURE 5-1
SOURCE/AMPLIFIER
POWER REF/DETECTED OUTPUT

5-25. Source/Amplifier Spurious Signal Check:

a. Connect A201J2 through a 30 dB, 1 watt attenuator to a spectrum analyzer.

b. Remove wire connected to A201FL1. Connect FL1 to a variable 0 to +8 VDC source. Vary the DC level to FL1 and observe the spectrum from 100 MHz to 400 MHz for spurious signals.

5-26. Front End Check:

a. Turn off counter power. Remove Converter tray (A2), and cover from IF Processor module (A204).

b. With Converter tray out of counter, reconnect tray to counter power at A200P1. Turn on power to counter.

c. Apply a signal in the 1 - 18 GHz range at +5 dBm to the Band B input connector.

d. Remove cable at A204J4 (Attenuator Control), then depress RESET button.

e. Monitor IF input at A204J8; a DC voltage between 50 to 250 mV should be indicated. If output is not in this range, either the Mixer (A205) or the Limiter/-Attenuator (A206) is faulty. CAUTION: Static discharge and/or voltage present at the input of some DVM's can damage the Mixer diode. Connect cables to test equipment, and discharge the center conductor before measuring the output at J8.

f. Re-install and reconnect above assemblies if OK.

5-27. Mixer Check:

a. Turn off counter power. Remove screws holding IF Processor (A204) to Converter tray (A2).

b. Remove co-ax inputs to Mixer (A205).

c. Unplug and remove IF Processor (A204).

d. Remove the two screws holding Mixer to IF Processor, and remove the Mixer.

e. Apply a 0 dBm signal in the 1 - 18 GHz range to the Mixer RF input port (see Figure 5-3). Monitor DC output with oscilloscope at IF converter port (connector that plugs into IF Processor). A DC voltage between 50 and 250 mV should be indicated.

f. Re-install and reconnect above assemblies if OK.

5-28. PIN Limiter/Attenuator Check:

a. Turn off counter power. Remove Converter tray (A2).

b. Remove PIN Limiter/Attenuator (A206) from tray.

c. Disconnect PIN Limiter/Attenuator from Converter Sequencer (A203). Unplug co-ax input to Mixer (A205).

d. Apply +7 VDC to A206P1 pin 4, and -8 VDC to A206P1 pin 1, with common to ground lug on module. CAUTION: Static discharge to these control input pins can damage the Limiter/Attenuator.

e. Apply a 0 dBm signal in the 1 - 18 GHz range to the type N connector. Output should be between -7 and -8 dBm.

f. Re-install and reconnect above assemblies if OK.

5-29. YIG Comb Generator Check:

a. Carefully remove co-ax cable connecting YIG Comb Generator output (A207J1) and Mixer (A205P1).

b. Connect a 1 - 18 GHz broadband calibrated detector to A207J1. The detector output should match Figure 5-2.

c. Check that the YIG Comb Generator (A207) has the proper inputs:

(1) 0 to 2 volt positive-going ramp at YIG Control A202J3 pin 5.

(2) RF power at A207J2 (from Source/Amplifier).

NOTE: Due to the special test equipment required to thoroughly test the performance of the YIG Comb Generator, the above check is adequate only as an indication of a complete failure.

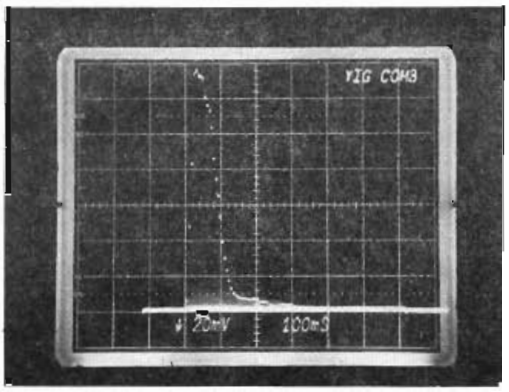


FIGURE 5-2
YIG COMB GENERATOR
DETECTED OUTPUT

EQUIPMENT DESCRIPTION	MFR	MODEL	Section 5 - Service	Section 6 - Calibration	Section 7 - Performance
Signal Source:					
(1) 300 MHz - 1.4 GHz	Wavetek	2001B	x	x	x
(2) 1 GHz - 18 GHz	S-D	521-series	x	x	x
(3) 300 MHz 18 GHz Pulse Modulator				x	x
Pulse Generator	IEC	P23		x	x
Oscilloscope: Dual Trace, 200 MHz Bandwidth	Tektronix	475	x	x	x
Digital Voltmeter (4½ digit)	Dana	4800	x	x	
Power Meter	HP	432B	x	x	x
Thermistor Mount (10 MHz-18 GHz)	HP	8478	x	x	x
Crystal Detector	HP	8472A		x	
20 dB Directional Coupler	HP	779D		x	
Variable 115 Vac Source	Staco	3PN501			x
Extender Card	EIP	2020021	x	x	
Adapter Cable (SMC to BNC)	EIP	2040015	x	x	
Misc. Attenuators, adapters, and cables			x	x	x

*See paragraphs 6-21 and 7-10.

TABLE 5-1
RECOMMENDED TEST EQUIPMENT

5-30. IF Processor Check:

a. Turn off counter power. Disconnect both co-ax inputs to Mixer (A205).

b. Remove IF Processor (A204) from Converter tray. Keep A204P1 (power plug) connected to A200J1.

c. Connect IF Processor to two signal generators as shown in Figure 5-3. Terminate A204J3 in 50 ohms.

d. Turn on counter.

(Signal Threshold Detector Check)

e. Connect oscilloscope 10X probe to A204J6 ($\overline{\text{Band B Threshold}}$).

f. Set LO signal source for 1 GHz ± 1 MHz at -16 dBm, and apply to LO Mixer port (see Figure 5-3).

g. Set RF signal source to 1.2 GHz. Vary RF level from -30 to -20 dBm. A204J6 should go low before RF level reaches -21 dBm.

(Converter Inhibit Check)

h. Set RF source to -20 dBm. Terminate A204J5 in 50 ohms.

i. Verify that A205J6 is at an ECL high (-0.8 VDC). Remove 50 ohm termination.

(Attenuator Control Check)

j. Connect oscilloscope Chan. A 10X probe to A204J4 (Attenuator Control), and Chan. B 10X probe to A204J1 (Converter Threshold).

k. Vary RF source level from below -20 dBm to above -10 dBm. Observe the following:

(1) When RF level is below -20 dBm, A204J1 (ECL level) and A204J4 (TTL level) are both high.

(2) As the level of the RF source is increased, A204J1 goes low. Note this level.

(3) A204J4 goes low 6 to 8 dB higher than A204J1 went low.

(In-Band Detector/Lock Logic Check)

l. Connect Channel A 10X probe to A204J7 (Lock).

m. Set RF source to -20 dBm with 1 kHz square wave modulation. Tune RF source from 1.4 GHz down to 1.0 GHz. Check that the Lock signal goes high (ECL level) at 1.327 GHz ± 3 MHz. *Note this frequency.*

n. Tune RF source from 1.0 GHz to 1.4 GHz. Check that the Lock signal goes high at 1.100 GHz ± 5 MHz, and then goes low at a frequency 25 to 30 MHz higher than that measured in step m above.

(Detected Modulation Check)

o. Set RF source to 1.2 GHz at -30 dBm. Modulate RF source with 1.5 microsecond pulses at a 20 kHz repetition rate.

p. Connect Channel A 10X probe to A204J2 (Detected Modulation). Output should be 1.5 microsecond positive pulses at 1.6 to 2.4 V amplitude (referenced to -6 volts).

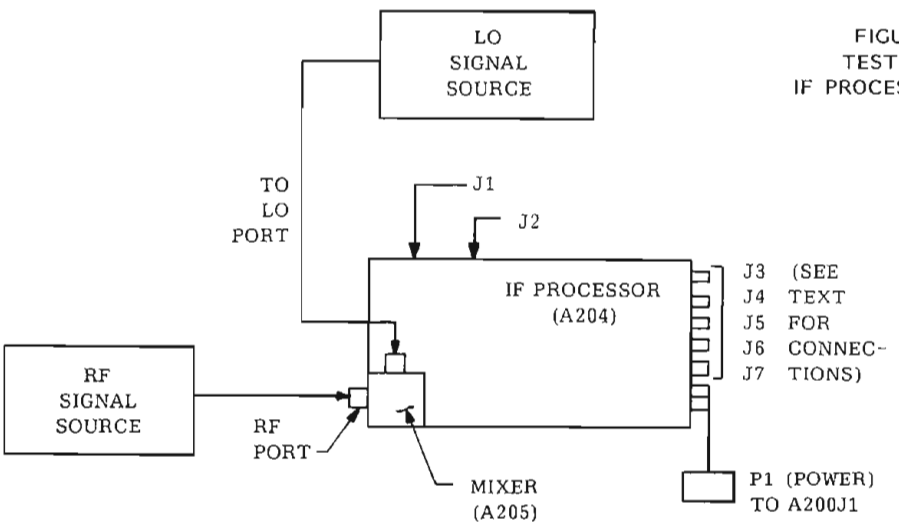


FIGURE 5-3
TEST SET-UP
IF PROCESSOR (A204)

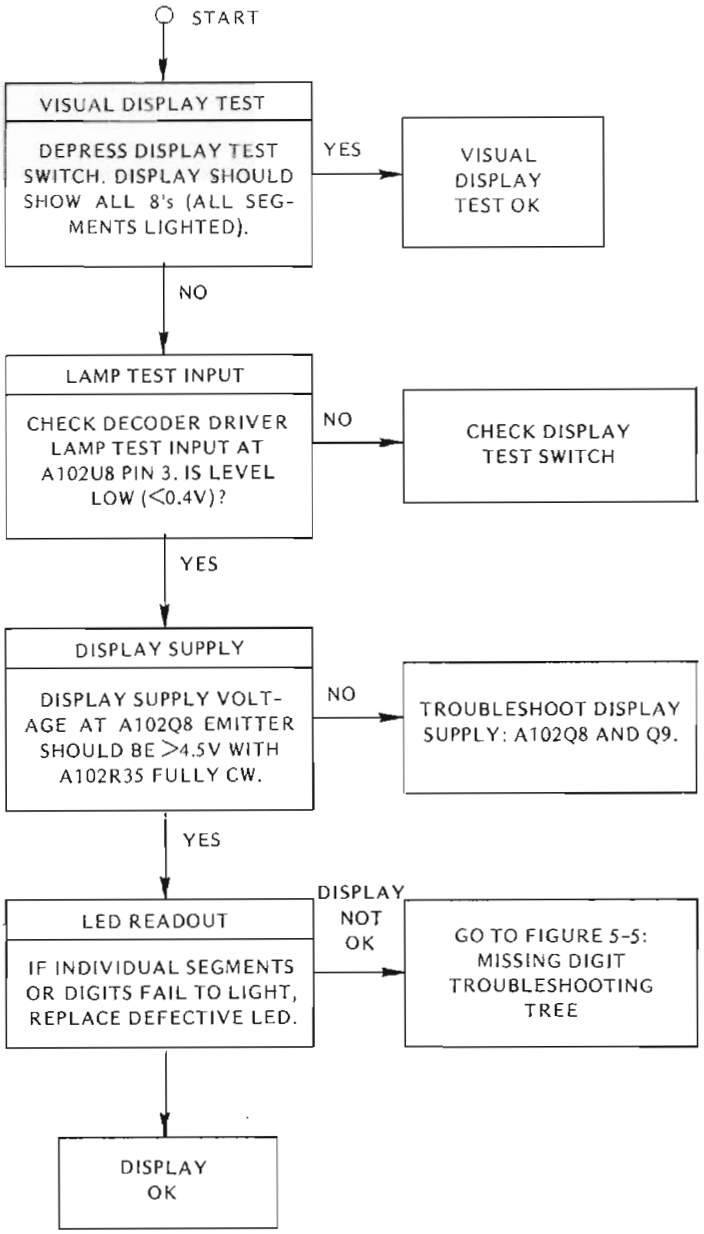


FIGURE 5-4
VISUAL DISPLAY TEST

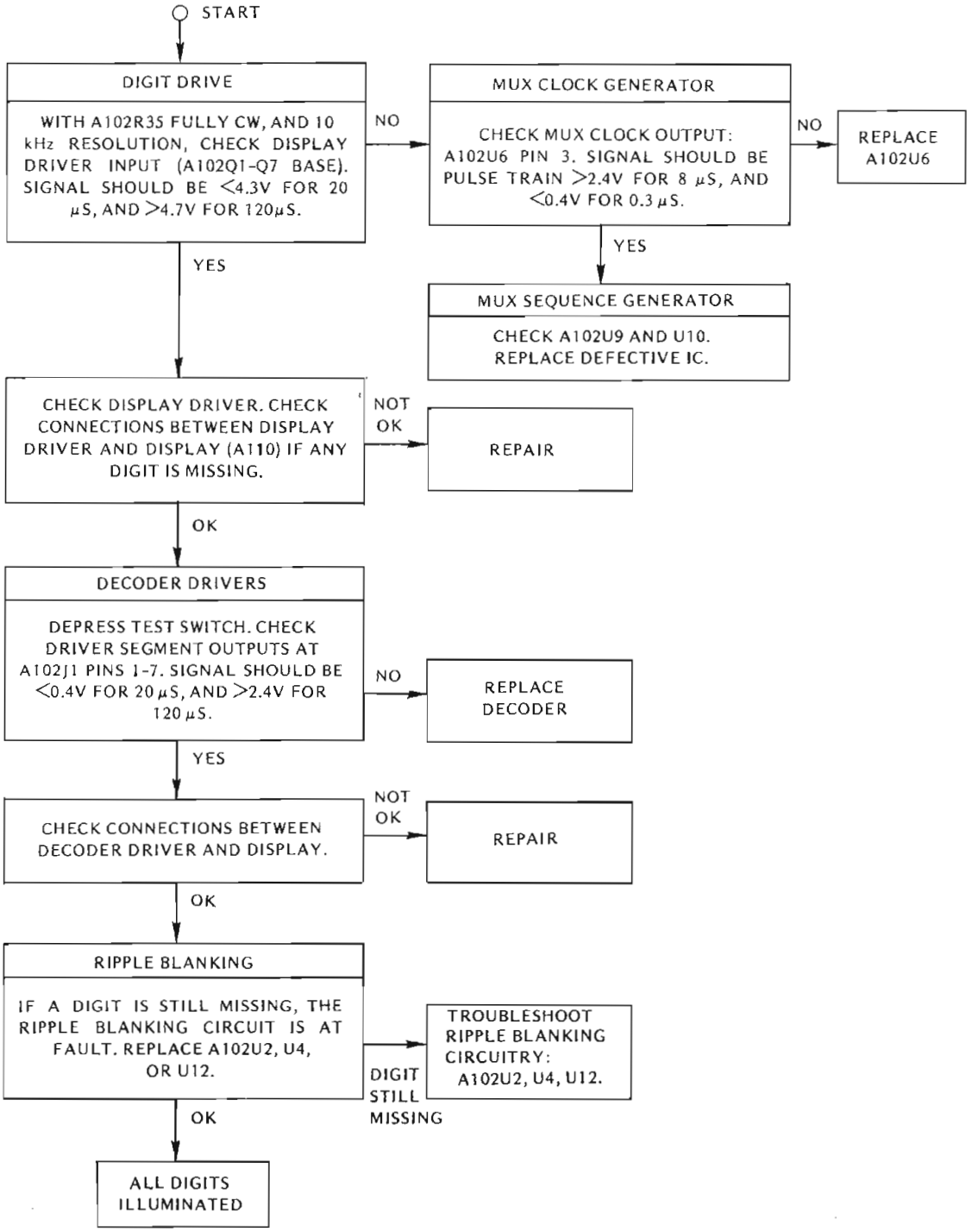


FIGURE 5-5
MISSING DIGIT

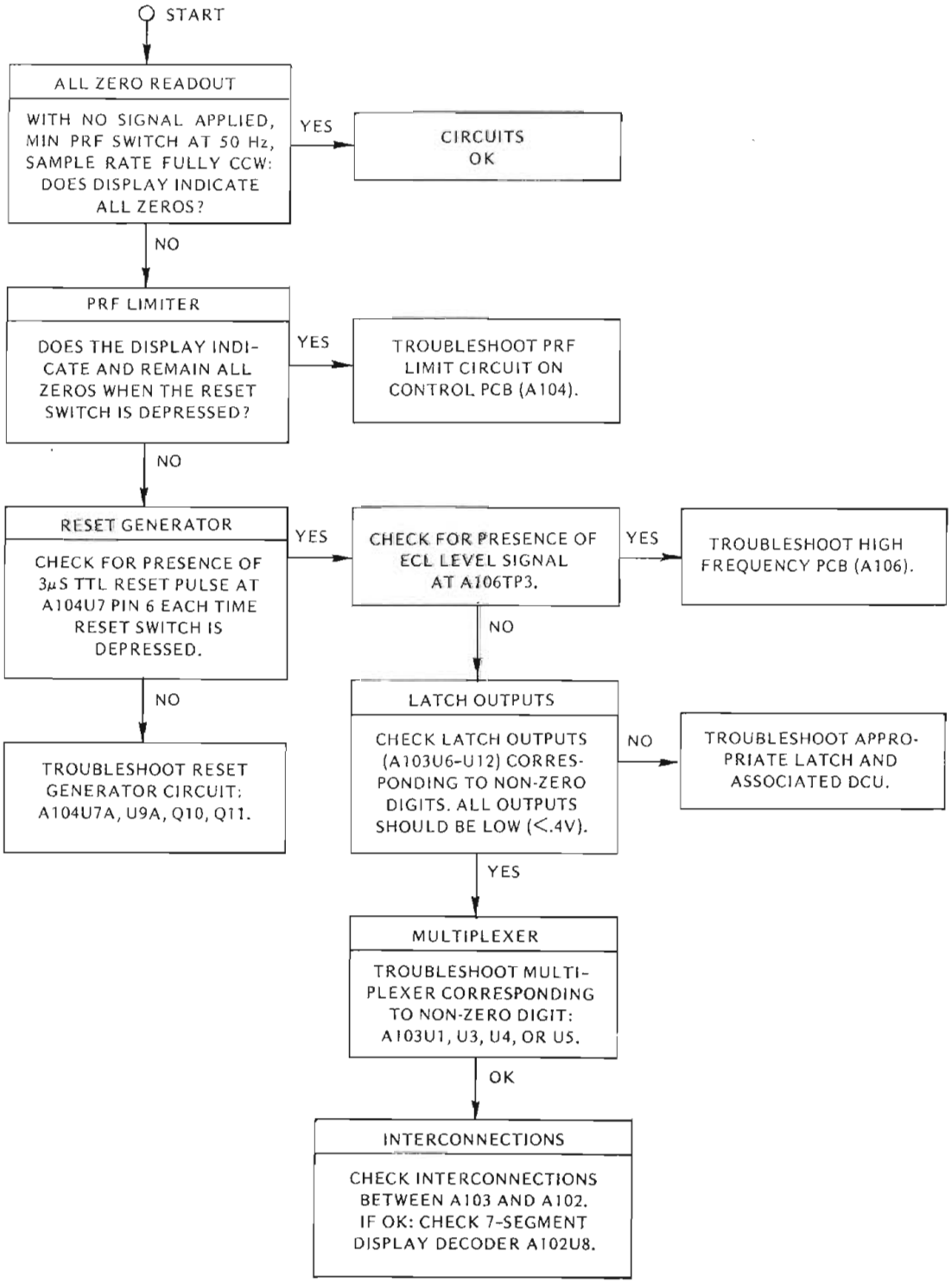
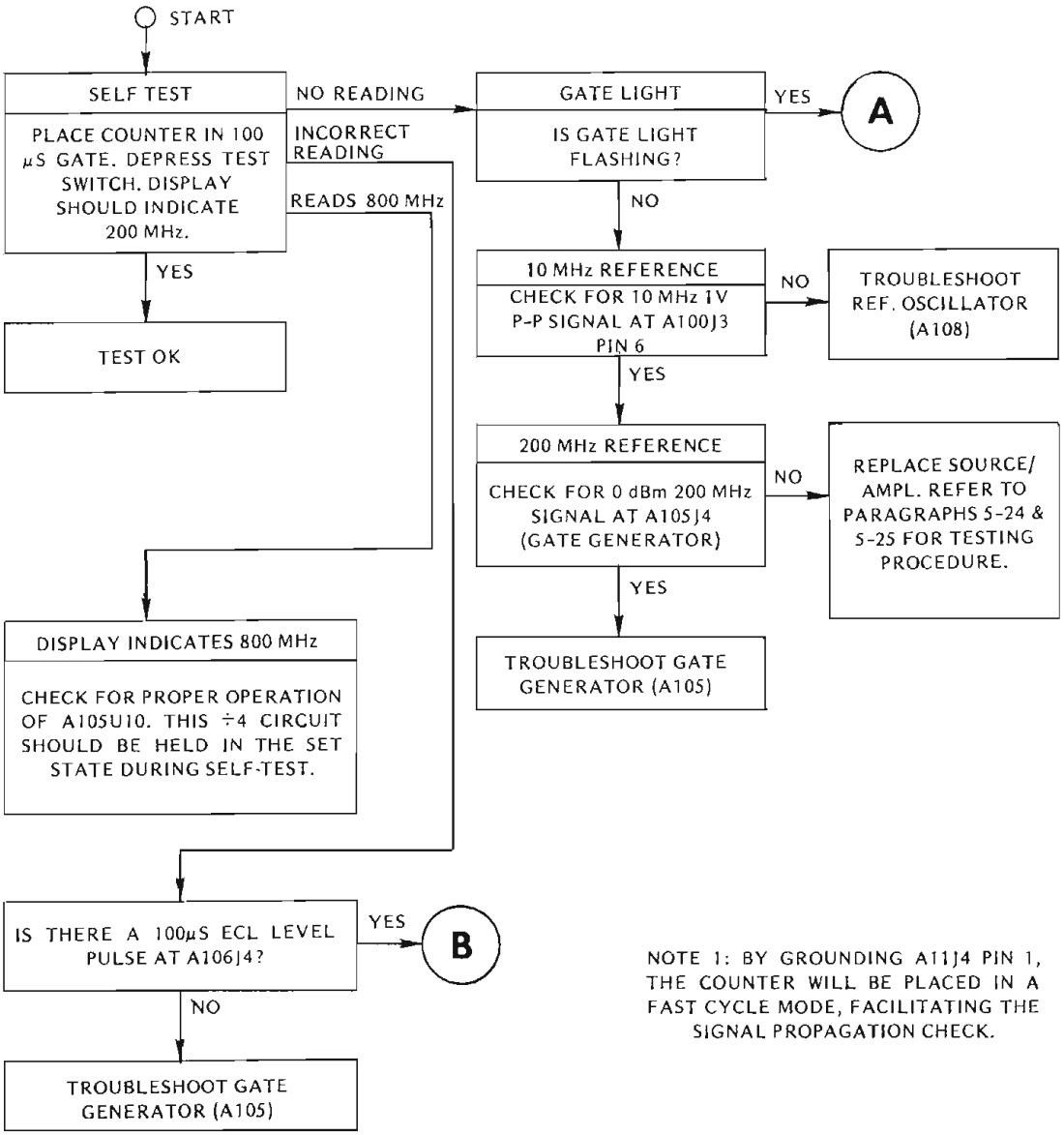


FIGURE 5-6
NON-ZERO DISPLAY



NOTE 1: BY GROUNDING A11J4 PIN 1, THE COUNTER WILL BE PLACED IN A FAST CYCLE MODE, FACILITATING THE SIGNAL PROPAGATION CHECK.

FIGURE 5-7
SELF-TEST

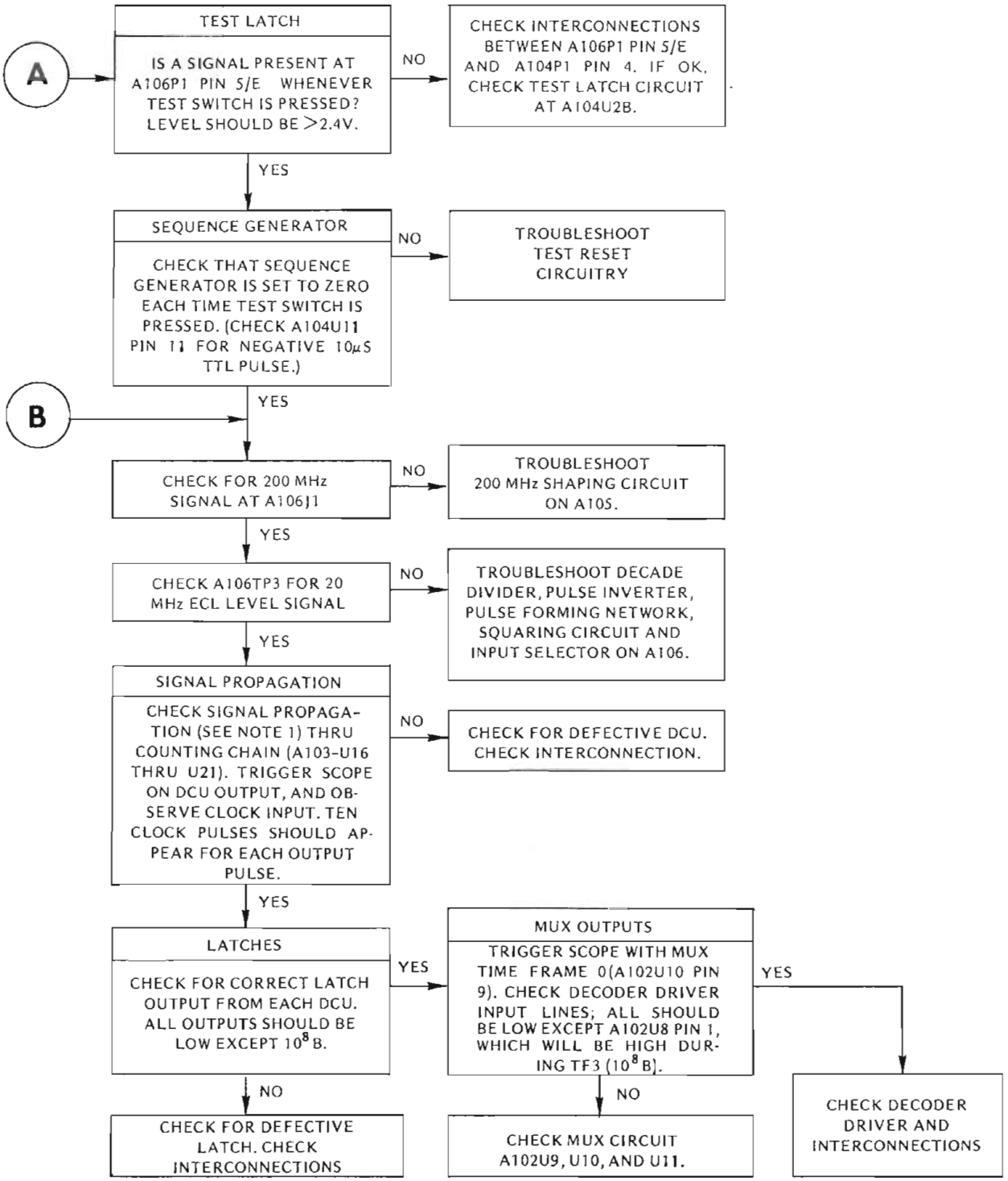


FIGURE 5-7
SELF-TEST
(Continued)

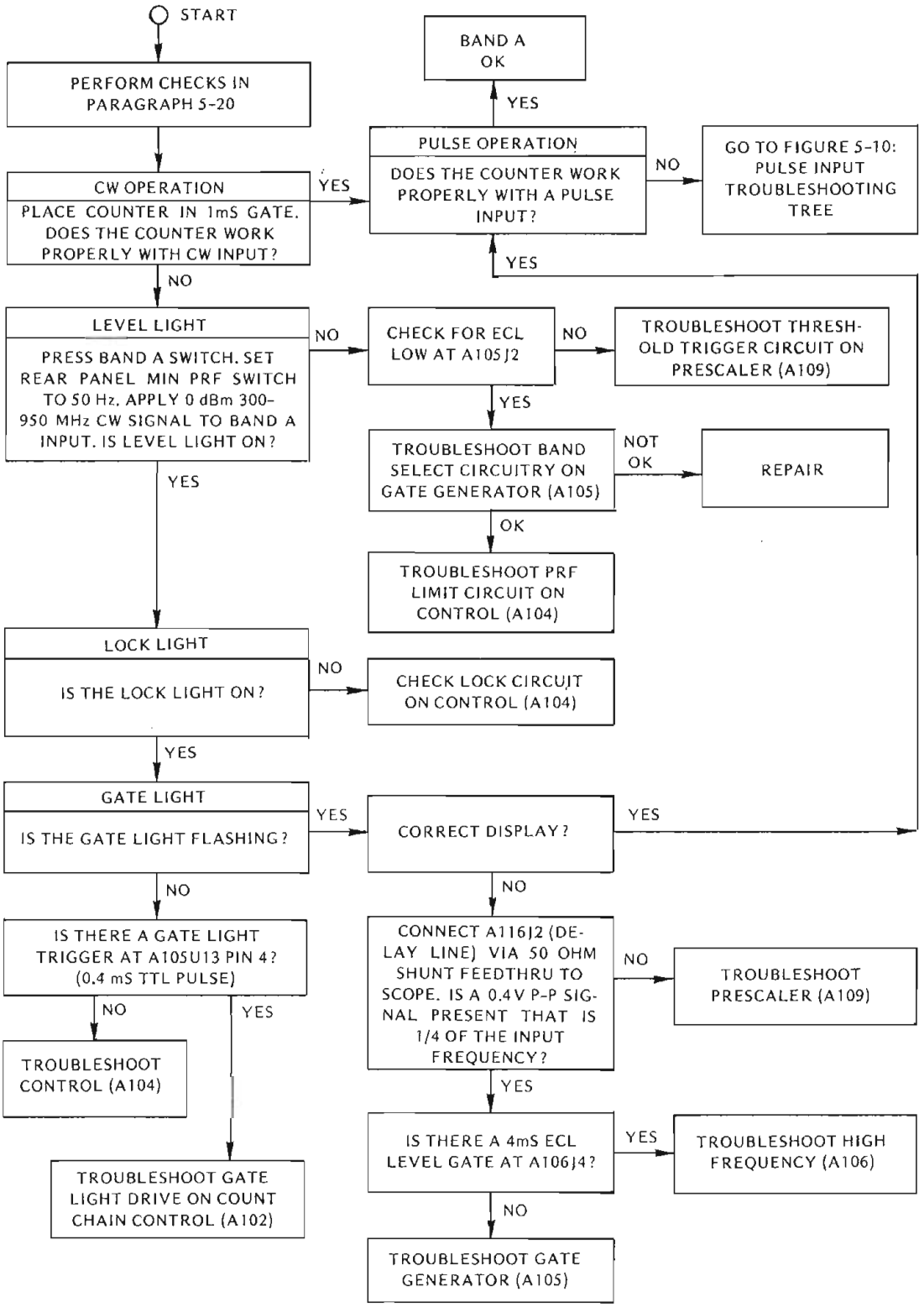


FIGURE 5-8
BAND A (OPT P2)
300 MHz - 950 MHz

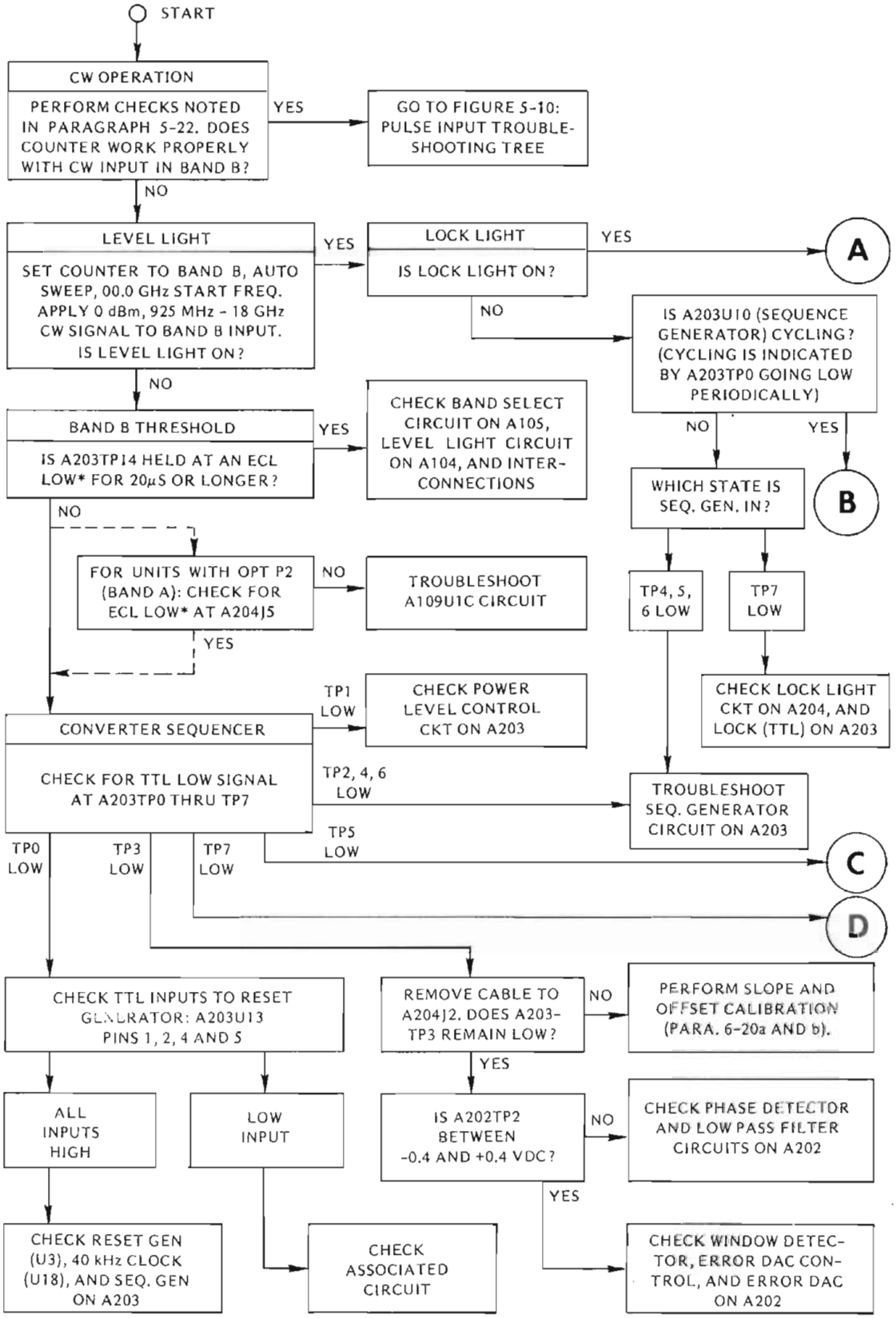


FIGURE 5-9
BAND B (CONVERTER)
925 MHz - 18 GHz

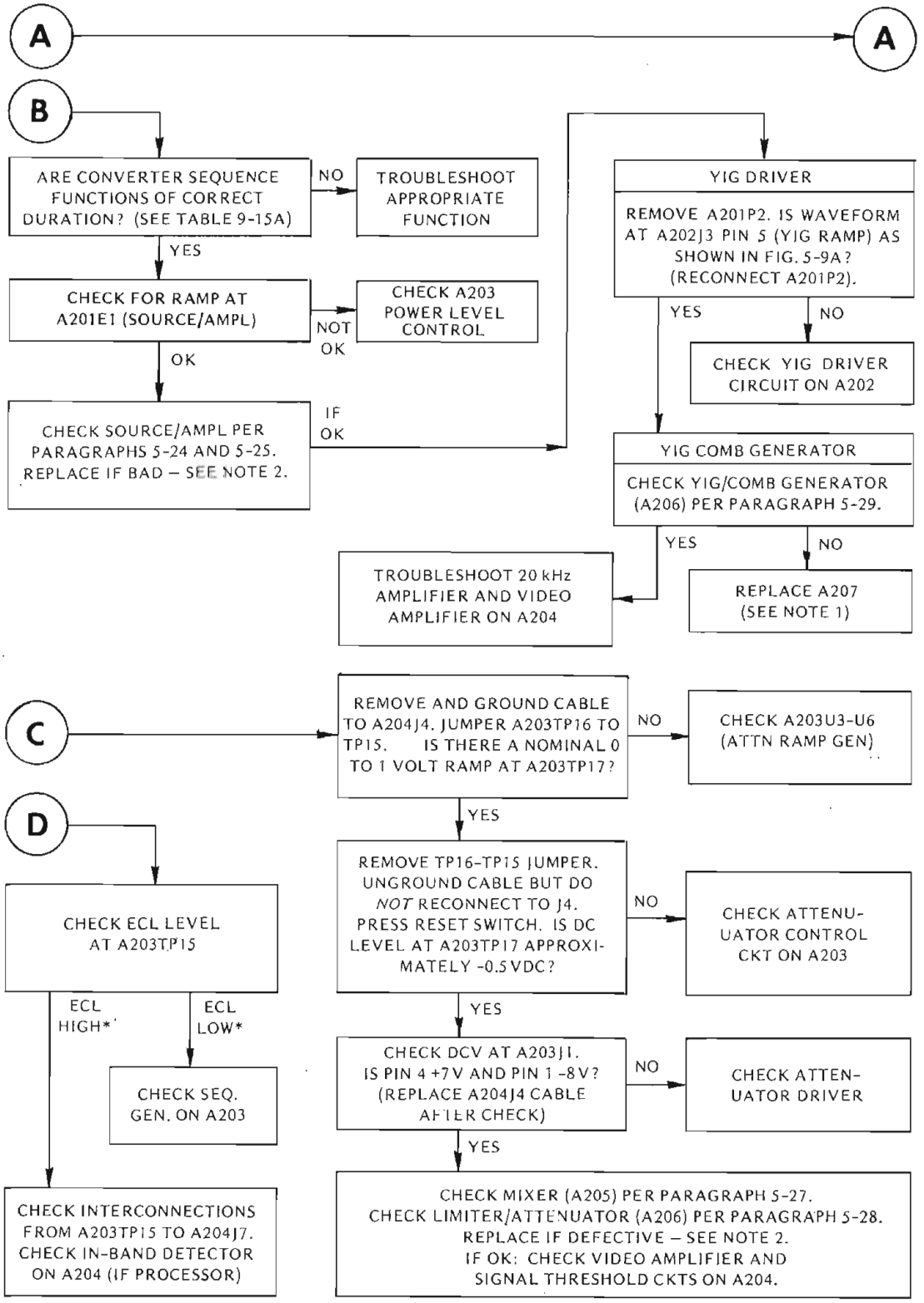
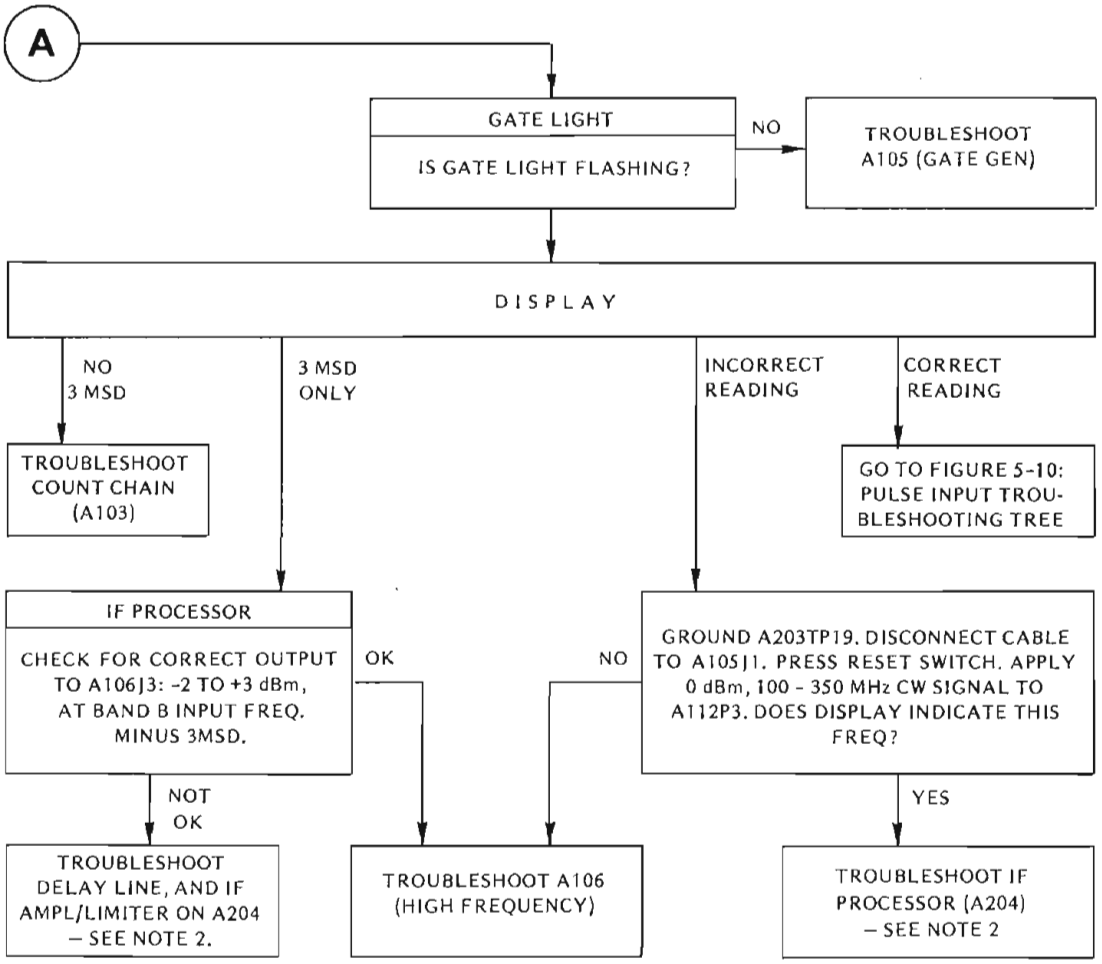


FIGURE 5-9
BAND B (CONVERTER)
925 MHz - 18 GHz (Continued)



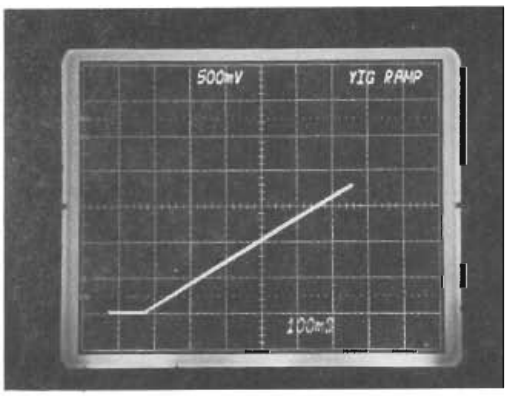


FIGURE 5-9A. YIG RAMP

* ECL HIGH = -0.8 VDC, ECL LOW = -1.7 VDC.

NOTE 1: THE FOLLOWING ASSEMBLIES SHOULD BE REPLACED, NOT REPAIRED, IF DEFECTIVE (SEE PARAGRAPH 5-9): A205 (MIXER), A206 (LIMITER/ ATTENUATOR), A207 (COMB GEN).

NOTE 2: THE FOLLOWING ASSEMBLIES REQUIRE SPECIAL CALIBRATION PROCEDURES AND SHOULD BE REPLACED, NOT REPAIRED, IF DEFECTIVE (SEE PARAGRAPH 5-9): A201 (SOURCE AMPLIFIER), AND A204 (IF PROCESSOR).

FIGURE 5-9
BAND B (CONVERTER)
925 MHz - 18 GHz (Continued)

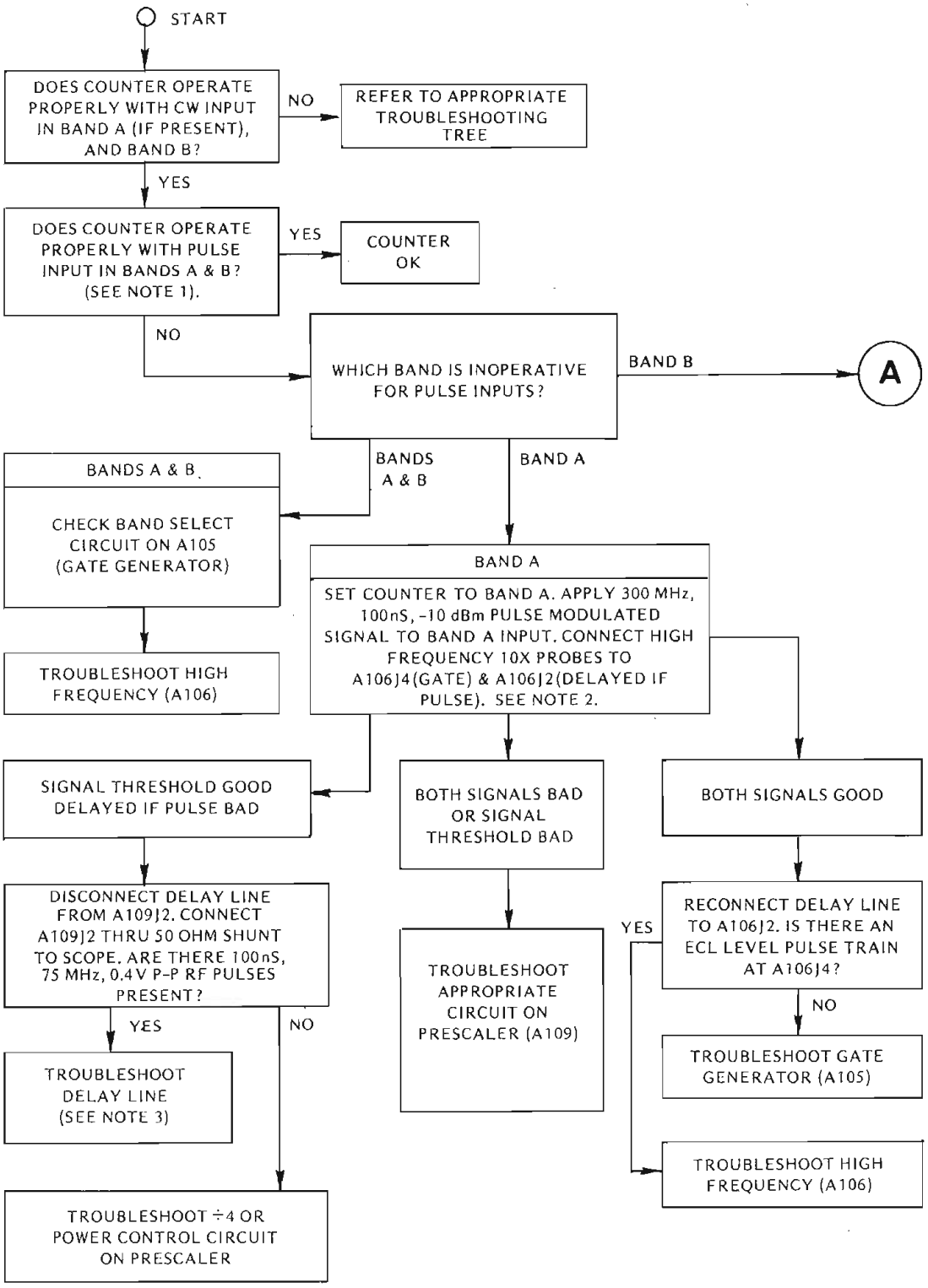
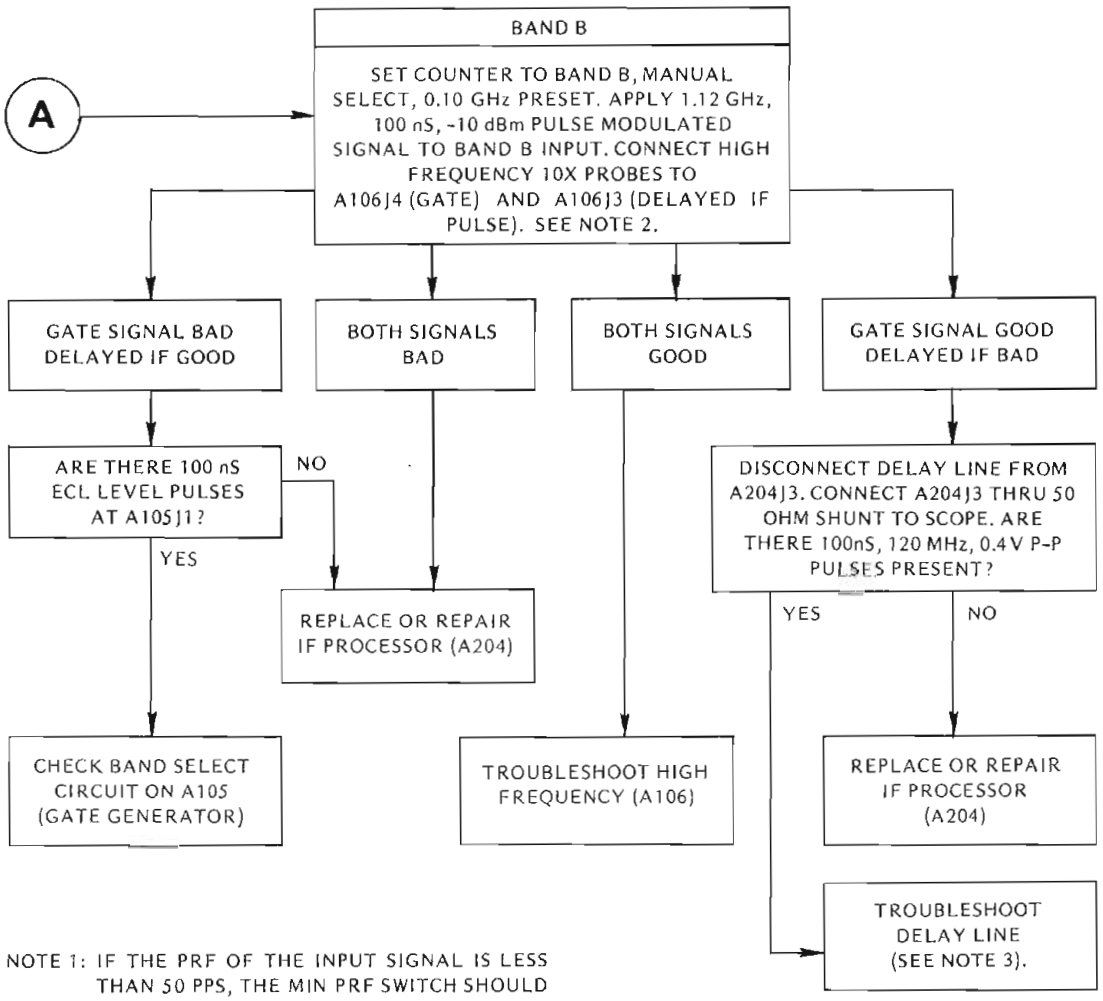


FIGURE 5-10
PULSE INPUT



NOTE 1: IF THE PRF OF THE INPUT SIGNAL IS LESS THAN 50 PPS, THE MIN PRF SWITCH SHOULD BE IN THE 0 Hz POSITION.

NOTE 2: IN ORDER TO MEASURE THE TRUE TIME RELATIONSHIP BETWEEN THE GATE AND DELAYED IF SIGNALS, IT WILL BE NECESSARY TO TAKE INTO CONSIDERATION THE DIFFERENCE IN TIME DELAY BETWEEN THE TWO CHANNELS OF THE OSCILLOSCOPE. REFER TO FIGURE 5-10A FOR WAVEFORMS, AND FIGURE 3-6 FOR TIMING DELAYS.

NOTE 3: DELAY LINE SPECIFICATIONS: IMPEDANCE: 50 OHMS. DELAY: 70 nS. ATTENUATION AT 100 MHz: 7 dBm, AT 300 MHz: 13 dBm. COUNTERS EQUIPPED WITH OPTION P2 (PRESCALER) HAVE TWO IDENTICAL DELAY LINES CONTAINED WITHIN ONE ASSEMBLY.

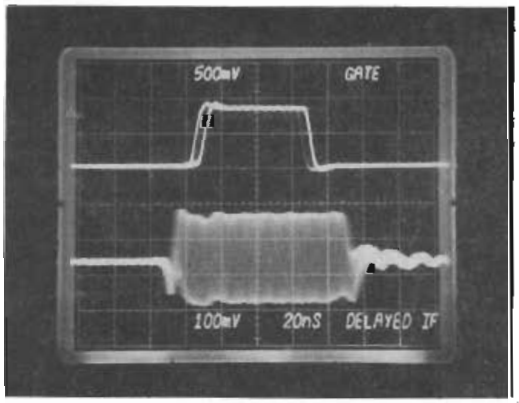


FIGURE 5-10A
DELAYED IF AND GATE SIGNALS

FIGURE 5-10
PULSE INPUT (Continued)

SECTION 6

ADJUSTMENTS & CALIBRATION

6-1. GENERAL

6-2. This section describes the procedures to be followed to correctly adjust the EIP 451 Microwave Pulse Counter. In general, adjustments should only be made if the instrument is not operating within specifications, or following replacement of components. Recommended test equipment is specified in Table 5-1. If adjustments do not result in specified performance, refer to Section 5.

6-3. GENERATING AND MEASURING NARROW RF PULSES

6-4. There are two potential problem areas that arise when generating narrow RF pulses by modulation of a CW source: (1) frequency pulling due to impedance changes in the modulator, and (2) video leakage of the modulating waveform.

6-5. The input impedance of a modulator generally varies with its state: on, off, or switching. This variation in loading will cause shifts in the frequency of the microwave source. The extent of this pulling effect is dependent upon the type of source, type of modulator, and the degree of isolation between them. Pulling of several megahertz for poorly isolated sources is not uncommon.

6-6. Modulators generally incorporate some form of fast switching diode, whose state is changed by the application of an appropriate bias current or voltage waveform. Coupling capacitors are used to separate the bias lines from the RF circuit. Video leakage is the transient signal caused by the modulating waveform being coupled into the RF lines. Usually this appears as a spike or ringing waveform at the leading and trailing edges of the modulating pulse. If care is not taken to provide adequate filtering, or otherwise eliminate this effect, significant measurement errors can occur, especially for fast rising pulses (less than 10 nanoseconds). On an unfiltered system, video leakage can exceed applied RF signals by several orders of magnitude.

6-7. In order to measure the peak power of an RF pulse, it will be necessary to use a calibrated crystal detector (such as the HP 8472A), a 50 ohm shunt feedthru to terminate the detector output, and a 50 MHz oscilloscope to observe the detected video pulse. The measurement is made by connecting the detector to the cable that normally feeds the Band A or B input of the counter, with the detector output fed through the shunt to the scope. The observed peak amplitude of the pulse is then compared to the calibration curve of the detector to find the peak pulse power. The 3 dB pulse width is the time interval between the points on the pulse waveform corresponding to one-half the peak power.

IMPORTANT

Many adjustments are dependent upon previous ones. It is essential that care be taken to perform adjustments in exactly the order presented below. Adjustment locations are shown in Figure 6-1.

6-8. POWER SUPPLY ADJUSTMENT

6-9. Prior to any power supply adjustments, the instrument should be allowed to warm-up for at least 20 minutes. All voltages are measured on Counter Interconnect board at A100P3. Adjust basic DC voltages as follows:

a. Connect DVM to ground at A100P3 pin 12.

b. Measure +12 VDC output. Adjust A107R7 until output is +12.000 ± .010 VDC.

c. Measure +5 VDC output. Adjust A107R15 until output is +5.000 ± .010 VDC.

d. Measure -12 VDC output. Adjust A107R21 until output is -12.000 ± .010 VDC.

e. Measure -5.2 VDC output. Adjust A107R31 until output is -5.200 ± .010 VDC.

6-10. TIME BASE CALIBRATION

IMPORTANT

The precision of time base calibration directly affects overall counter accuracy. Reasons for recalibration, and procedures to be used, should be thoroughly understood before attempting any readjustment.

6-11. The fractional frequency error in the frequency indicated by the counter, is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\Delta f_s}{f_s} = - \frac{\Delta f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus the inaccuracy associated with a frequency meas-

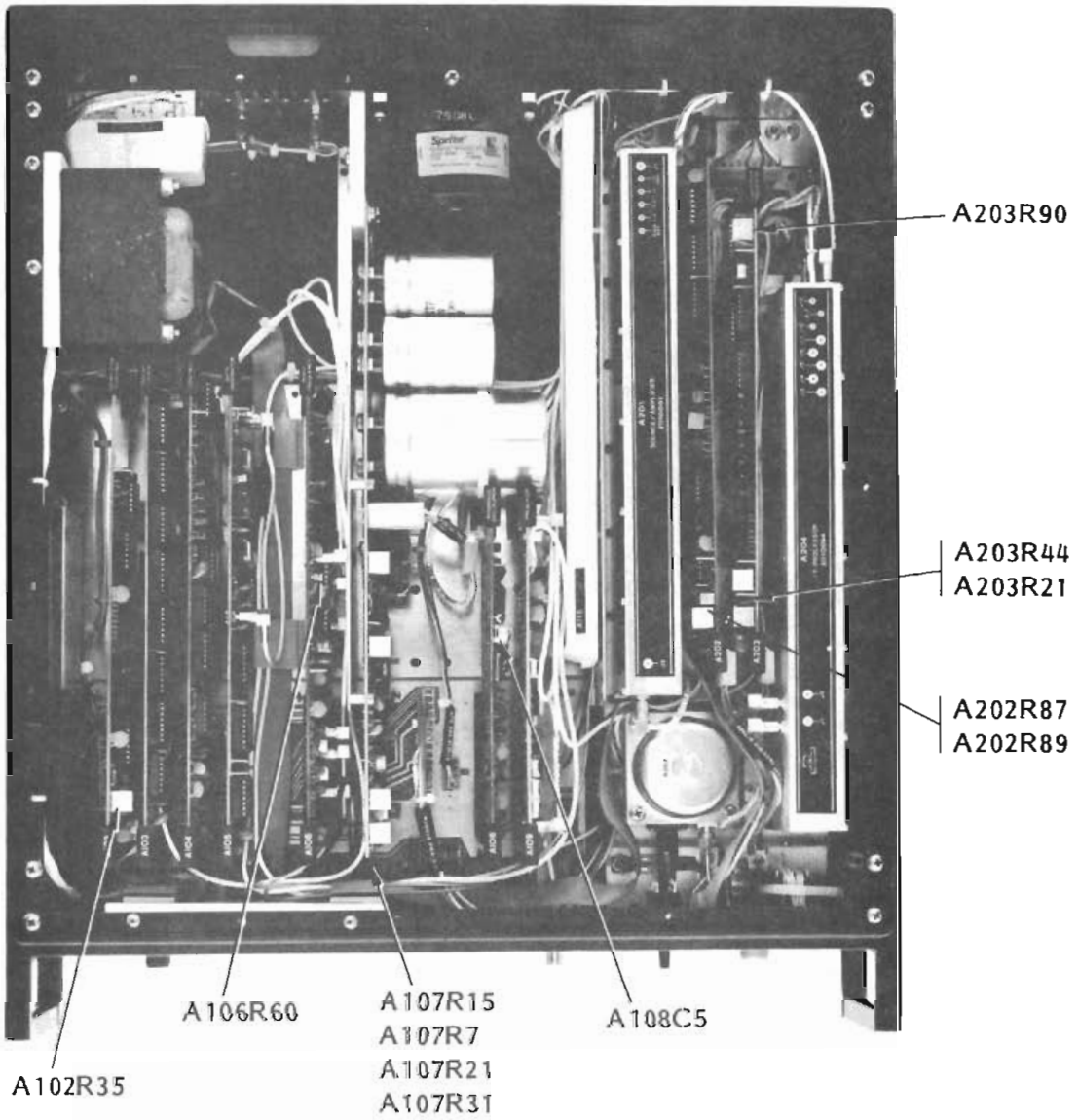


FIGURE 6-1
CALIBRATION
ADJUSTMENT
LOCATOR

urement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

6-12. RTO CALIBRATION PROCEDURE

a. Measure the frequency of the RTO (Room Temperature Crystal Oscillator) at the rear panel 10 MHz OUT connector with a second counter of known accuracy.

b. Adjust the RTO (if necessary) by turning A108C5 until the measured frequency is 10 000 000 ± 5 Hz.

6-13. TCXO CALIBRATION (OPTION P1)

6-14. Option P1 consists of a temperature-compensated crystal oscillator (TCXO) mounted in place of the RTO on Oscillator board A108. The highest and lowest actual measured TCXO frequencies will differ by no more than 2 parts in 10^6 if the temperature is varied slowly from 0° to +50°C. Therefore, an indicated measurement will exhibit the same fluctuation even though the signal being measured is not changing. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side, the frequency to which it must be set at +25°C. The calibration procedure for this adjustment is described in paragraph 6-18.

6-15. At approximate room temperature (+25°C), the slope of the frequency vs.temperature curve, is normally no worse than -1×10^{-7} parts per °C. Therefore, if the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10 000 000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5°C will result in a measured signal error due to oscillator temperature characteristics of no more than $\pm 2.5 \times 10^{-7}$ parts.

6-16. Another source of inaccuracy in the measured signal due to the Time Base Oscillator originates in the natural aging characteristic of the crystal. Aging refers to the long term, irreversible change in frequency, generally in the positive direction, which all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is specified to be less than 3×10^{-7} parts per month. This may be expected to improve in time to be no worse than 1×10^{-6} parts per year in continuous service.

6-17. Error due to aging adds directly to error due to temperature perturbations. Thus the frequency of recalibration is dependent upon the overall accuracy requirement of the counter and its environment. For example: If the counter is subjected to the full operating temperature range and initially adjusted properly, then one month later the inaccuracy over temperature could be expected to vary from $+ 1.3 \times 10^{-6}$ parts, to $- 0.7 \times 10^{-6}$ parts.

6-18. TCXO CALIBRATION PROCEDURE

a. Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

b. Measure the frequency of the TCXO at the rear panel 10 MHz OUT connector with a second counter of known calibration accuracy.

c. Adjust the TCXO (if necessary) by turning the calibration screw on the TCXO case until the measured frequency is the same as that shown on the TCXO calibration label.

6-19. BAND A (OPTION P2) ADJUSTMENTS (300 MHz to 950 MHz)

a. If the High Frequency board (A106) is repaired or replaced, perform the adjustments given in paragraph 6-22. No other Band A adjustment is required.

6-20. BAND B ADJUSTMENTS (925 MHz to 18 GHz)

a. 40 kHz Clock Adjustment

NOTE: Required only upon replacement of YIG Comb Generator (A207), or Converter Sequencer board (A203).

(1) Set A203R90 fully ccw (counter-clockwise).

(2) Set counter to Band B, MANUAL SELECT, and 01.0 GHz PRESET FREQUENCY.

(3) Jumper A202TP1 to TP3. Ground A202TP5.

(4) Connect oscilloscope Channel A to A202U1 pin 9, and Channel B to A202U1 pin 4.

(5) Adjust A202R89 for a symmetrical waveform as shown in the upper trace of Figure 6-2. (All pulses in the train should be of equal duration.)

(6) If necessary, select a new value for A203R93 so the leading and trailing edges of the 20 kHz reference (lower trace) occur in the center of the detected modulation pulses. (If A203R93 is changed, readjust A202R89 as stated in (5) above.)

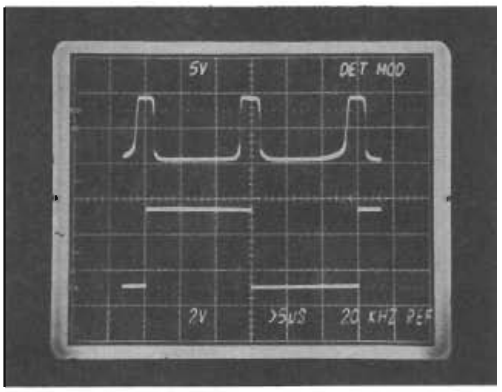


FIGURE 6-2
DETECTED MOD/20 kHz
REFERENCE PULSE TIMING

b. Slope and Offset Adjustments

(1) Repeat paragraph 6-20a(1) through (5).

(2) Change preset in 1 GHz steps from 1 to 18 GHz, adjusting A202R87 to produce a symmetrical waveform across the band.

(3) Repeat steps (1) and (2) above as necessary.

(4) Remove jumper from A202TP1 and TP3. Remove ground from A202TP5.

c. Attenuator Driver Adjustments

NOTE 1: These adjustments are difficult to make, and require careful set-up by personnel familiar with microwave return loss measurements. These adjustments affect only the Band B input VSWR of the counter, and should be made only: (1) when it is known that there is excessive input VSWR, (2) the attenuator driver on A203 has been repaired, or (3) if A203 or A206 have been replaced.

NOTE 2: To make a meaningful return loss measurement, use a directional coupler with a minimum directivity of at least 25 dB (Example: HP 779D).

(1) Set counter to Band B, AUTO SWEEP, 00.0 GHz START FREQUENCY.

(2) Carefully set-up equipment as shown in Figure 6-3. Note especially where cables or adapters must not be used (which would degrade accuracy of the adjustment).

(3) Set Limiter/Attenuator (A206) to maximum insertion loss, by connecting a jumper between A203-TP16 and TP21.

(4) Adjust A203R44 for maximum return loss (waveform will be a DC level).

NOTE 3: As R44 is rotated from full ccw to full cw, the amplitude observed on the scope will go from a maximum point through a minimum point and then to a maximum again. Maximum return loss (minimum reflected signal) occurs at the minimum point.

(5) Remove jumper from A203TP16 to TP21.

(6) Cycle Limiter/Attenuator (A206) through its normal operating range by removing and grounding the cable to A204J4.

(7) Inhibit the counter from locking up by jumpering A203TP14 to TP16.

(8) Connect an 0.47uf capacitor across A203C2.

(9) Trigger scope from A203TP17 (Attenuator Control Ramp).

(10) Adjust A203R21 for maximum return loss. See Note 3, and Figure 6-4 for typical waveform.

(11) Remove jumper between A203TP14 and TP16. Remove capacitor. Reconnect cable to A204J4.

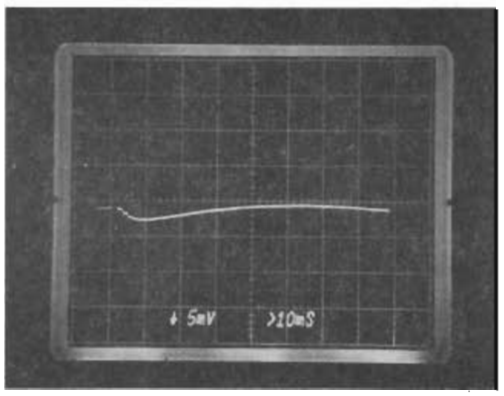


FIGURE 6-4
RETURN LOSS MEASUREMENT

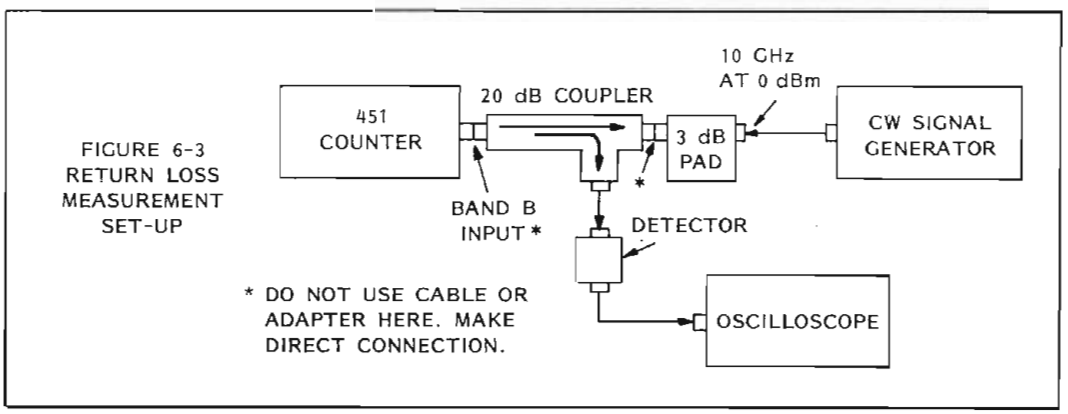


FIGURE 6-3
RETURN LOSS
MEASUREMENT
SET-UP

d. Attenuator Control Adjustments

NOTE: To be performed only upon installation of a new Limiter/Attenuator (A206), or replacement of the Converter Sequencer board (A203).

(1) Connect an 0.47uf capacitor across A203C2.

(2) Connect the Channel A 10X probe of scope to A203J1 pin 1 (I_{series}). Connect Channel B 10X probe to A203TP17.

(3) Remove and ground cable to A204J4.

(4) Connect jumper between A203TP14 and TP16.

(5) Select a value for A203R18 so the first two or three steps of the Attenuator Control Ramp have no effect upon I_{series} (see Figure 6-5).

(6) Remove jumper between A203TP14 and TP16. Remove capacitor. Reconnect cable to A204J4.

(7) Apply a 0 dBm, 1.4 GHz CW signal to Band B input.

(8) Press RESET switch. Increase signal level to the Band B input until the REDUCE SIGNAL light comes on. (Light should come on between +4 and +6 dBm. If it does not, select a new value for A203-R17, and repeat steps (7) and (8) until it does.)

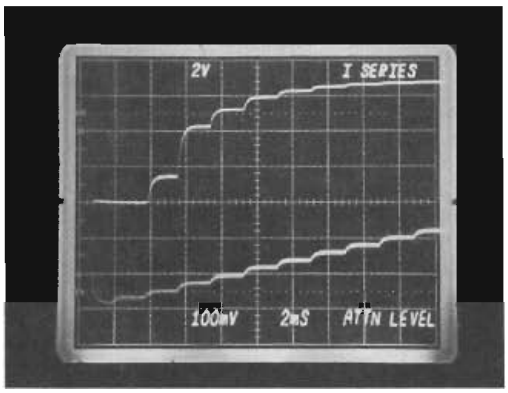


FIGURE 6-5
ATTENUATOR CONTROL
RAMP OFFSET ADJUSTMENT

e. Comb Leveling

(1) Set-up counter as described in paragraph 6-20c(1).

(2) Jumper A203TP14, TP15, and TP16 together.

(3) Connect Channel A 10X scope probe to A203-TP12. Trigger scope from A203TP20 (Reset).

(4) Press RESET switch.

(5) Adjust A203R64 to level comb lines to 1 volt nominal (see Figure 6-6).

(6) Remove jumpers from TP14, TP15, and TP16.

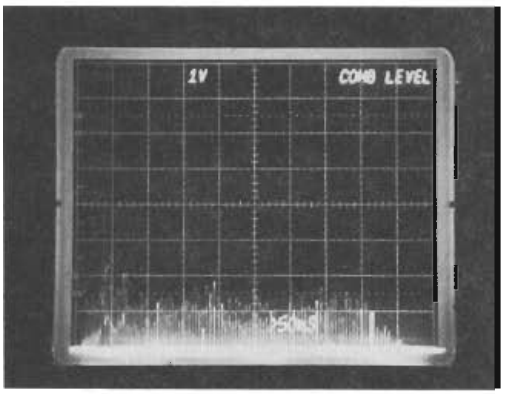


FIGURE 6-6
COMB LEVELING

6-21. HIGH FREQUENCY (A106) ADJUSTMENTS

a. Gate Accuracy — Band A (Option P2):

(1) Set-up counter and perform error measurement as described in paragraph 7-10.

(2) Adjust A106R60 to minimize difference between averaged pulse reading and CW reading.

NOTE: If using Method A, it will be necessary to (a) have a stable RF source that will not be pulled more than 10 kHz while being modulated by a 100 nS pulse, (b) have no video information on the RF pulse, and (c) have a means of measuring RF pulse width and amplitude. Also, when using Method A, adjust A106R60 so the average pulse reading is centered about the CW reading (gate error equal to zero).

b. Gate Accuracy — for counters NOT equipped with Band A (Option P2):

(1) Set SAMPLE RATE control fully counter-clockwise, BAND SELECT to Band B, MANUAL SELECT, and 0.10 PRESET FREQUENCY.

(2) Apply a 1.3 GHz CW signal at -10 dBm to the Band B input.

(3) Adjust A106R60 per paragraph 6-21a(2).

SECTION 7

PERFORMANCE TESTS

7-1. GENERAL

7-2. The purpose of this section is to enable the user to verify that the counter meets specifications over the entire frequency range, with both CW and pulse inputs. NOTE: For the verification of specifications not included in this section, please consult the factory.

7-3. VARIABLE LINE VOLTAGE

7-4. During the performance tests, the counter should be connected to the power source through a variable voltage device, so line voltage can be varied ± 10% from nominal (100/120 or 220/240 VAC), to assure proper operation of the counter under various supply conditions.

7-5. RECOMMENDED TEST EQUIPMENT

7-6. Refer to Table 5-1 for recommended test equipment. Other equipment may be used provided that performance is equal to, or better than, that listed in the table.

7-7. PERFORMANCE TESTS

7-8. RANGE, SENSITIVITY, AND MINIMUM PULSE WIDTH — BAND A (OPTION P2) (300 MHz to 950 MHz)

a. Set SAMPLE RATE control fully counter-clockwise, and BAND SELECT switch to Band A.

b. Connect a CW signal source to the Band A input.

c. Vary source frequency from 300 MHz to 950 MHz at -10 dBm. Counter should display correct frequency.

d. Connect a 100 nanosecond pulse modulated signal source to the Band A input. Set level to -10 dBm. Vary source frequency from 300 MHz to 950 MHz. Counter should display correct frequency. NOTE: Refer to paragraph 6-3 for pulse width measurement.

7-9. RANGE, SENSITIVITY, AND MINIMUM PULSE WIDTH — BAND B (925 MHz to 18 GHz)

a. Set SAMPLE RATE control fully counter-clockwise, BAND SELECT switch to Band B, AUTO SWEEP, and 00.0 GHz START FREQUENCY.

b. Connect a CW leveled source to the Band B input.

c. Vary source frequency from 925 MHz to 18 GHz at the following levels:

925 MHz - 10 GHz: -10 dBm
10 GHz - 18 GHz: -5 dBm

Counter should display the correct frequency.

d. Connect a 100 nanosecond pulse modulated signal source to the Band B input. Repeat step c above. NOTE: Refer to paragraph 6-3 for pulse width measurement.

7-10. GATE ERROR — BAND A (OPTION P2)

NOTE: Refer to paragraph 3-34 for discussion of gate error.

a. Set SAMPLE RATE control fully counter-clockwise, and BAND SELECT switch to Band A.

b. Apply a 950 MHz CW signal at -10 dBm to the Band A input.

NOTE: Gate error readings can be taken using two modulation methods (A or B), and two measurement methods: strip chart (most accurate method) or scratch pad.

Modulation Methods:

METHOD A: Pulse modulates signal source with 100 nS wide, negative-going ECL level pulses.

METHOD B: Simulates modulation by applying 100 nS wide ENABLE pulses to INPUT INHIBIT connector on counter rear panel. (This method is preferred as it avoids errors associated with possible pulling of the signal source.)

c. Error Measurement Using Strip Chart Recorder:

(1) Set-up test equipment as shown in Figure 3-7, with recorder connected to the BCD output of the counter.

(2) Record the CW frequency reading.

(3) Pulse modulate — use Method A or B.

(4) Record the average pulse reading.

(5) Gate error is equal to the difference between the reading for (2) and (4). For 100 ns wide pulses, error should be less than 1.42 MHz.

d. Error Measurement Using Scratch Pad:

(1) Reduce SAMPLE RATE time so each reading can be recorded on scratch pad or chart.

(2) Record CW frequency reading.

(3) Pulse modulate — use Method A or B.

(4) Record and then average ten or more successive readings.

(5) Gate error is equal to the difference between the readings for (2) and (4). For 100 ns wide pulses, error should be less than 1.42 MHz

7-11. GATE ERROR — BAND B

NOTE: Refer to paragraph 3-34 for discussion of gate error.

a. Set SAMPLE RATE control fully counter-clockwise, BAND SELECT to Band B, AUTO SWEEP, and 01.0 GHz START FREQUENCY.

b. Apply a 1.3 GHz CW signal at -10 dBm to the Band B input.

c. Repeat step 7-10c. Repeat step 7-10c. Gate error should be less than 570 kHz. NOTE: Gate error is a function of IF frequency.

7-12. REAR PANEL OUTPUT LEVELS

a. Apply a pulse modulated signal to the counter.

b. Measure GATE and SIGNAL THRESHOLD outputs using a 50 ohm shunt feedthru to an oscilloscope.

(1) SIGNAL THRESHOLD OUTPUT should be zero VDC with no RF signal, and at least -0.5 VDC when RF is present.

(2) GATE OUTPUT should be at least - 0.5 VDC, corresponding to counter gate.

7-13. REAR PANEL INPUT INHIBIT LEVELS

NOTE: INPUT INHIBIT has a 50 ohm source impedance returned to -2 VDC.

a. Apply a CW signal to the counter.

b. Apply -1.7 VDC to the INPUT INHIBIT connector. Counter should operate normally.

c. Apply - 0.9 VDC to the INPUT INHIBIT connector. Counter should stop counting, and operate as if a no signal condition existed.

SECTION 8

PARTS LISTS

8-1. GENERAL

8-2. This section contains information helpful in ordering replacement parts for this counter. Four tables provide sufficient information for identifying a part and obtaining a replacement, either from EIP or from the manufacturer.

8-3. LIST OF TABLES

a. Table 8-1, REFERENCE DESIGNATORS/ABBREVIATIONS: Lists abbreviations used as schematic reference designators, and in parts list descriptions. Note that some components have two distinct "codes" identifying that part. For example: an integrated circuit is identified on schematics as "U", but in the parts lists as "IC".

b. Table 8-2, LIST OF MANUFACTURERS: Provides a listing of manufacturers names and addresses, and their Federal Supply Code for Manufacturers (FSCM) number. The FSCM number (or an equivalent) is used in the parts lists as the guide to the manufacturer or supplier of the part.

c. Table 8-3, MASTER PARTS LIST: This list has an entry for each separate replaceable part used in the counter. Entries are arranged by EIP Part Number and contain a part description plus the manufacturer's part and FSCM number. This table is used with Table 8-4 to completely identify a component part.

d. Table 8-4, REPLACEABLE PARTS LIST: This table provides a detailed component parts listing for all PC boards and assemblies where the parts or components are field replaceable. NOTE: Certain assemblies cannot be field repaired, but must be returned to EIP for service. This table is arranged first by Assembly number (A101, A102, etc.), then by the schematic reference designator (if any) associated with the assembly. Parts identical to those listed earlier for that assembly are identified in the column headed "SAME". The EIP Part Numbers refer to those listed in Table 8-3.

8-4. TO ORDER REPLACEMENT PARTS:

a. Send order directly to EIP at the address shown on the title page of this manual.

b. Specify the EIP Part Number, Reference Designator (if any), and a brief description of the part.

c. For parts not listed in the Parts List: Specify the function, location, and description of the part required, and the model and serial number of the counter.

TABLE 8-1.
REFERENCE DESIGNATORS AND ABBREVIATIONS

REFERENCE DESIGNATORS

A	Assembly
B	Battery or Fan
C	Capacitor
CR	Diode
DS	Indicator (display)
F	Fuse
J	Jack or Connector
K	Relay
L	Inductor
P	Plug or PCB contacts
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
U	Integrated Circuit
W	Wire (cable)
X	Socket or Holder
Q1-3	Q1 through Q3
Q1/2	Q1 and Q2 (matched pair)

ABBREVIATIONS

CAP	Capacitor
CBN	Carbon
CER	Ceramic
CMT	Cermet
CNTR	Counter
CONV	Converter
COMP	Composition
CONN	Connector
DI	Diode
ELEC	Electrolytic
FDTH	Feedthrough
FLM	Film
FML	Female
GP	General Purpose
IC	Integrated Circuit
K	Kilo (x 1,000)
LED	Light-emitting-diode
M	Meg (x 1,000,000)
MET OX	Metal Oxide
MF	Metal Film
MH	Millihenry
ML	Male
MTCH PR	Matched Pair
PC	Printed Circuit
PCB	PC Board Assembly
PF	Picofarad
PREC	Precision
RSTR	Resistor
RT AN	Right Angle
S.A.T.	Value or type selected during factory test. Part may not be used.
SW	Switch
TANT	Tantalum
TRIM	Trimmer
UF	Microfarad
UH	Microhenry
VAR	Variable
WPRF	Waterproof
WW	Wirewound
XSTR	Transistor

FSCM	MFR NAME,ADDRESS,ZIPCODE
00809	CROVEN LTD,WHITBY,ONTARIO,CANADA
01121	ALLEN-BRADLEY CO.,SO.MILWAUKEE,WI 53204
01295	TEXAS INSTRUMENTS INC.,DALLAS,TX 75222
02660	AMPHENOL CONNECTOR DIV.,BUNKER RAMO CORP.,BROADVIEW,IL 60153
02735	SOLID STATE DIV.,RCA CORP.,SOMERVILLE,NJ 08876
04009	ARROW-HART INC.,HARTFORD,CT 06106
04618	AMERICAN PAMCOR INC.,PAOLI,PA 19301
04713	SEMICONDUCTOR DIV.,MOTOROLA INC.,PHOENIX,AZ 85008
05245	CORCOM INC.,CHICAGO,IL 60639
05591	GENERAL RESISTANCE DIV.,CHRONETICS INC.,MT.VERNON,NY 10550
07263	FAIRCHILD SEMICONDUCTOR, MOUNTAIN VIEW,CA 94040
08717	SLOAN COMPANY,SUN VALLEY,CA 91352
09353	C AND K COMPONENTS INC.,WATERTOWN,MA 02172
11236	CTS OF BERNE INC.,BERNE,IN 46711
12436	GENERAL DYNAMICS CORP.,SAN DIEGO,CA 92112
14298	AMERICAN COMPONENTS INC.,CONSHOHOCKEN,PA 19428
14433	ITT SEMICONDUCTOR DIV.OF ITT CORP.,W.PALM BEACH,FL 33401
18324	SIGNETICS CORP.,SUNNYVALE,CA 94086
18518	MSI ELECTRONICS INC.,WOODSIDE,NY 11377
21793	DANA LABORATORIES INC.,IRVINE,CA 92664
23880	STANFORD APPLIED ENGINEERING INC.,SANTA CLARA,CA 95050
23936	PAMOTOR INC.,BURLINGAME,CA 94010
24546	CORNING GLASS WORKS,BRADFORD,PA 16701
26654	VARADYNE INDUSTRIES,SANTA MONICA,CA 90404
27014	NATIONAL SEMICONDUCTOR CORP.,SANTA CLARA,CA 95051
28480	HEWLETT-PACKARD CO.,PALO ALTO,CA 94304
29990	ATC DIV,PHASE INDUST,HUNTINGTON STATION,NY 11746
50522	ELECTRONIC SPECIAL PRODUCTS,MONSANTO CO.,CUPERTINO,CA 95014
56289	SPRAGUE ELECTRIC CO.,NORTH ADAMS,MA 01247
70903	BELDEN CORP.,CHICAGO,IL 60644
71400	BUSSMAN MFG DIV.,MCGRAW-EDISON CO.,ST.LOUIS,MO 63107
72136	ELECTRO-MOTIVE MFG. CO.,WILLIMANTIC,CT 06226
72259	NYTRONICS INC.,PELHAM MANOR,NY 10803
72982	ERIE TECHNOLOGICAL PRODUCTS INC.,ERIE,PA 16512
73138	HELIPOT DIV.,BECKMAN INSTRUMENTS,FULLERTON,CA 92634
73445	AMPEREX ELECTRONIC CORP.,HICKSVILLE,NY 11802
80031	MEPCO/ELECTRA INC.,MORRISTOWN,NJ 07960
81349	MILITARY SPECIFICATION
86797	ROGAN BROS.INC.,SKOKIE,IL 60076
91637	DALE ELECTRONICS INC.,COLUMBUS,NE 68601
91836	KINGS ELECTRONICS CO.,TUCKAHOE,NY 10707
95275	VITRAMON INC.,BRIDGEPORT,CT 06601
98291	SEALECTRO,MAMARONECK,NY 10544
99800	DELAVAN DIV.,AMERICAN PRECISION INDUST.,EAST AURORA,NY 14052
	FOLLOWING MFRS DO NOT HAVE FSCM NUMBER
0000A	MOLEX INC.,LISLE,IL 60532
0000B	STETTNER-TRUSH,CAZENOVIA,NY 13035
0000C	PLESSEY ELECTRO-PRODUCTS,LOS ANGELES,CA 90066
0000L	R-OHM CORPORATION,IRVINE,CA 92664
0000M	LEMO U.S.A. INC.,BERKELEY,CA 94710
0000X	ANY MANUFACTURER OF THIS PRODUCT

TABLE 8-2. LIST OF MANUFACTURERS

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
2020041	PCB:UNIVERSAL EXTENDER	EIP	
2030002	OSC,XTAL: TCXO	EIP	SRCE CONT DWG
2030011	OSC,XTAL: ROOM TEMP	00809	A187DED-30
2030013	OSC,XTAL: 5.185 MHZ	EIP	SRCE CONT DWG
2040063	ASSY:HARNESS	EIP	451-A110
2040066	ASSY:HARNESS	EIP	451-A204
2040068	ASSY:HARNESS	EIP	451-A200
2040073	ASSY:CABLE,FLT RIBBON	EIP	451-A110
2040090	ASSY:CABLE,FLEX,CO-AX	EIP	451-A103
2040091	ASSY:CABLE,FLEX,CO-AX	EIP	451-A105
2040092	ASSY:CABLE,FLEX,CO-AX	EIP	451-A105
2040095	ASSY:CABLE,FLEX,CO-AX	EIP	451-A200
2040096	ASSY:CABLE,FLEX,CO-AX	EIP	451-A200
2040097	ASSY:CABLE,FLEX,CO-AX	EIP	451-A200
2040098	ASSY:CABLE,FLEX,CO-AX	EIP	451-A200
2040099	ASSY:CABLE,FLEX,CO-AX	EIP	451-A200
2040107	ASSY:CABLE,FLEX,CO-AX	EIP	451-A109
2040112	ASSY:HARNESS	EIP	
2100002	CAP:CHIP .001UF 20% 50V	95275	VJ1210A102MF
2100010	CAP:CHIP 10PF 10% 50V	95275	VY73CA100KF
2100011	CAP:CHIP 10PF 5% 50V	29990	ATC100A100JC50
2150001	CAP:CER .001UF 20% 1KV	56289	5GA-D10
2150003	CAP:CER .01UF 20% 100V	56289	TG-S10
2150005	CAP:CER .02UF 20% 100V	56289	TG-S20
2150010	CAP:CER .05UF 20V	71590	UK20-503
2150012	CAP:CER .1UF 16V	0000R	RT-16-0.1Z
2160004	CAP:CER 10PF NPO 500V	72982	301000C0H0100C
2160005	CAP:CER 12PF NPO 500V	72982	301000C0G0120C
2160006	CAP:CER 15PF NPO 500V	72982	301000C0G0150J
2160007	CAP:CER 18PF NPO 500V	72982	301000C0G0180J
2160008	CAP:CER 2.2PF NPO 500V	72982	301000C0J0229C
2160009	CAP:CER 22PF NPO 500V	72982	301000C0G0220J
2160010	CAP:CER 24PF NPO 500V	72982	301000C0G0240J
2160011	CAP:CER 3.0PF NPO 500V	72982	301000C0J0309C
2160012	CAP:CER 3.3PF NPO 500V	72982	301000C0J0339C
2160013	CAP:CER 4.7PF NPO 500V	72982	301000C0H0479C
2160014	CAP:CER 6.8PF NPO 500V	72982	301000C0H0689C
2160016	CAP:CER 20PF NPO 500V	72982	301000C0G0200J
2160999	CAP:CER-SELECT AT TEST	72982	301000C0X0XXXX
2200010	CAP:ELEC 8500UF 25V	80031	91S25HA852
2200011	CAP:ELEC 40000UF 15V	80031	91S15JB44
2200012	CAP:ELEC 11000UF 15V	80031	39CS15JP113
2250001	CAP:MICA 10PF 5% 500V	72136	DM15CD100D0
2250002	CAP:MICA 100PF 5% 500V	72136	DM15CD101JO
2250003	CAP:MICA 1000PF 5% 500V	72136	DM15CD102JO
2250005	CAP:MICA 150PF 5% 500V	72136	DM15CD151JO
2250006	CAP:MICA 180PF 5% 500V	72136	DM15CD181JO
2250008	CAP:MICA 20PF 5% 500V	72136	DM15CD200JO
2250009	CAP:MICA 200PF 5% 500V	72136	DM15CD201JO
2250010	CAP:MICA 22PF 5% 500V	72136	DM15CD220JO
2250011	CAP:MICA 220PF 5% 500V	72136	DM15CD221JO
2250012	CAP:MICA 27PF 5% 500V	72136	DM15CD270JO
2250014	CAP:MICA 33PF 5% 500V	72136	DM15CD330JO
2250016	CAP:MICA 39PF 5% 500V	72136	DM15CD390JO
2250017	CAP:MICA 47PF 5% 500V	72136	DM15CD470JO
2250024	CAP:MICA 30PF 5% 500V	72136	DM15CD300JO
2250025	CAP:MICA 68PF 5% 500V	72136	DM15CD680JO
2250026	CAP:MICA 680PF 5% 500V	72136	DM15CD681JO
2250027	CAP:MICA 120PF 5% 500V	72136	DM15CD121JO
2250028	CAP:MICA 15PF 5% 500V	72136	DM15CD150JO
2250999	CAP:MICA-SELECT AT TEST	72136	DM15CDXXXXO
2300005	CAP:TANT .47UF 35V	14433	TAG20-0.47/35-50
2300008	CAP:TANT 1.0UF 35V	14433	TAG20-1.0/35-50
2300010	CAP:TANT 10UF 16V	14433	TAG20-10/16-50
2300015	CAP:TANT 33UF 10V	14433	TAG20-33/10-50
2300017	CAP:TANT 47UF 6.3V	14433	TAG20-47/6.3-50
2300020	CAP:TANT .10UF 35V	14433	TAG20-.10/35-50
2300023	CAP:TANT 33UF 20% 20V	14433	TAG20-33/20
2300024	CAP:TANT 100UF 20% 6.3V	14433	TAG20-100/6.3
2300025	CAP:TANT 47UF 20% 16V	14433	TAG20-47/16-20
2350001	CAP:TRIM 2-8PF 250V	00008	10S-T-22-2/8
2350002	CAP:TRIM 5.5-18PF 250V	00008	10S-T-22-5.5/18
2350003	CAP:TRIM 8-25PF 250V	00008	10S-T-22-8/25
2350017	CAP,FOTH:RF FILTER,5KPF	04618	859556-1
2350022	CAP:TRIM 5.5-18PF 250V	00008	10S-T-24-5.5/18
2350027	CAP:MONO .022UF 10% 50V	26654	2130X7R050R223K
2610010	CONN:JACK,BLKHD,RECPT	98291	51-045-0000
2610017	CONN:PLUG,PC RCPT,STR	98291	52-052-0000
2610018	CONN:JACK,PC RCPT,STR	98291	51-051-0000
2610024	CONN:BNC,BLKHD,TRS FNSH	91836	KC-79-35

TABLE 8-3. MASTER PARTS LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
2620005	CONN:PC WAFER 6PIN ML	0000A	09-18-5061
2620008	CONN:PC RT AN 5PIN ML	0000A	09-66-1051
2620014	CONN:PC WAFER 4PIN, ML	0000A	09-60-1041
2620016	CONN:PC WAFER, 6PIN, ML	0000A	09-60-1061
2620018	CONN:PC EDGE 18PIN	04618	1-583407-8
2620019	CONN:PC EDGE 8PIN	04618	583407-9
2620029	CONN:PC RT AN,3PIN, ML	0000A	09-66-1031
2620042	CONN:PC WAFER, 9PIN, ML	0000A	09-60-1091
2620044	CONN:PC WAFER,12PIN, ML	0000A	09-60-1121
2620048	CONN:PC RT AN 8PIN ML	0000A	09-66-1081
2630002	SOCKET: 16 PIN,NYLON	0000A	A-4497-16
2630003	SOCKET: 14 PIN,NYLON	0000A	A-4497-14
2640004	CONN 50PIN	02660	57-40500
2640022	CONN:RECPT,6 PIN,ML/FML	0000M	RA1,306NYL
2650003	CONN/FILTER:PANEL MNT	05245	6J4
2700827	DIODE: 6.2V ZENER	04713	1N827
2704001	DIODE: RECT	04713	1N4001
2704154	DIODE: GEN PURP	07263	1N4154
2704757	DIODE: 51V ZENER	04713	1N4757
2705227	DIODE: 3.6V ZENER	04713	1N5227
2705230	DIODE: 4.7V ZENER	04713	1N5230
2705231	DIODE: 5.1V ZENER	04713	1N5231
2705234	DIODE: 6.2V ZENER	04713	1N5234
2705237	DIODE: 8.2V ZENER	04713	1N5237
2710004	DIODE: HOT CARR	07263	FH1100
2710006	DIODE: HOT CARR	28480	5082-2800
2710012	DIODE:VOLT VAR CAP	04713	MV109
2710014	DIODE,MTCH PR:FH1100	EIP	2710004
2710016	DIODE: HOT CARRIER	28480	5082-2835
2710028	BRDG RECT	04713	MDA990-1
2710029	BRIDE RECT	04713	MDA970-1
2710030	DIODE,MTCH PR: MV1404	18518	HA116
2710031	DIODE,GRADED:1N960B-01	EIP	2730960
2710032	DIODE,GRADED:1N960B-02	EIP	2730960
2720963	DIODE: 12V ZENER	04713	1N963A
2800001	LAMP,INDICATOR: RED	50522	MV5021
2800004	IC:NUMERIC IND, RED	28480	5082-7730
2800008	LAMP,LED: GREEN	50522	MV5253
2800010	LAMP:LED,5V 15MA,RED	08717	2L5S-RTPFL5/15
2800014	LAMP:LED,YEL DIFFUSED	50522	MV5353
3007400	IC:QUAD 2INP NAND GATE	0000X	7400N
3007402	IC:QUAD 2INP NOR GATE	0000X	7402N
3007404	IC:HEX INVERTER	0000X	7404N
3007405	IC:HEX INVERTER	0000X	7405N
3007408	IC:QUAD 2INP AND GATE	0000X	7408N
3007410	IC:TRI 3INP NAND GATE	0000X	7410N
3007413	IC:DUAL 4INP NAND TRIG	0000X	7413N
3007420	IC:DUAL 4INP NAND GATE	0000X	7420N
3007430	IC:8INPUT NAND GATE	0000X	7430N
3007432	IC:QUAD 2INP OR GATE	0000X	7432N
3007447	IC:BCD/7SEG DECODER	0000X	7447N
3007454	IC:4WIDE 2INP AOI GATE	0000X	7454N
3007473	IC:DUAL J-K F/F	0000X	7473N
3007475	IC:QUAD LATCH	0000X	7475N
3007476	IC:DUAL J-K F/F	0000X	7476N
3007486	IC:QUAD 2INP EXCL OR GT	0000X	7486N
3007490	IC:DECADE COUNTER	0000X	7490N
3007493	IC:4BIT BINARY COUNTER	0000X	7493N
3007495	IC:4BIT SHIFT REGISTER	0000X	7495N
3009602	IC:DUAL TTL/MONOSTBL MV	0000X	9602N
3010616	IC:UHF COUNTER-DIVIDE/4	0000C	SP8616B
3010637	IC:UHF BCD DEC CNTR	0000C	SP8637B
3011414	IC:DUAL DIFF COMP	0000X	1414L
3011495	IC:FOUR-QUAD MULTIPLIER	0000X	1495L
3013440	IC:QUAD GPIB TRANSCVR	0000X	3440P
3013441	IC:QUAD GPIB TRANSCVR	0000X	3441P
3014044	IC:PHASE/FREQ DETECTOR	0000X	4044P
3040304	IC:VOLT REG	0000X	304
3040305	IC:VOLT REG	0000X	305
3040555	IC:TIMER,LINEAR	0000X	555V
3040733	IC:DIFF VIDEO AMPL	0000X	733
3040741	IC:OP AMPL	0000X	741CN
3041458	IC:OP AMPL	0000X	1458P1
3043049	IC:DUAL/DIFF AMPL	0000X	3049T
3043130	IC:OP AMPL: COS/MOS	0000X	3130S
3050005	IC:HEX INVERTER	18324	8T93A
3050311	IC:VOLT COMPARATOR	0000X	311N
3050710	IC:VOLT COMPARATOR	0000X	710CN
3054002	IC:RAM/4BIT OUTPUT PORT	34649	P4002-1
3054040	IC:4-BIT CPU	34649	C4040
3054201	IC:CLOCK GENERATOR	34649	P4201
3054265	IC:PGRM GP I/O DEVICE	34649	P4265
3054308	IC:ROM/4-BIT I/O PORTS	34649	P4308
3070001	IC:QUAD 2-1 LN DATA SEL	0000X	74LS257N
3070002	IC:QUAD BI-STABLE LATCH	0000X	74LS75P
3070003	IC:TTL/MONOSTABLE MV	0000X	74L123P
3070004	IC:S IN/P OUT 8BIT SR	0000X	74L164P
3070005	IC:P/S IN/S OUT 8BIT SR	0000X	74L165P
3070006	IC:QUAD 2INP NOR GATE	0000X	74LS02P
3070007	IC:QUAD 2/1 MULTIPLEXR	0000X	74L157P
3070008	IC:QUAD 2/1 MUX INV OUT	0000X	74S158P
3070009	IC:DUAL D F/F	0000X	74LS74P

TABLE 8-3 (Continued). MASTER PARTS LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
3070010	IC:QUAD 2INP NAND GATE	0000X	74L00N
3074123	IC:TTL/MONOSTABLE MV	0000X	74123N
3074155	IC:DUAL 2/4LINE DECODR	0000X	74155N
3074157	IC:QUAD 2INP MULTIPLEXR	0000X	74157N
3074176	IC:PRESET DEC COUNTER	0000X	74176N
3074177	IC:PRESET BINARY CNTR	0000X	74177N
3074193	IC:UP/DN BINARY CNTR	0000X	74193N
3074196	IC:PST DECADE COUNTER	0000X	74196N
3074279	IC:QUAD RS LATCH	0000X	74279P
3074393	IC:DUAL 4-BIT BIN CNTR	0000X	74393P
3074490	IC:DUAL DECADE CNTR	0000X	74490P
3090003	IC:DUAL 4INP AND GATE	0000X	74H21N
3090004	IC:TRIP 3INP AND GATE	0000X	74H11P
3110102	IC:QUAD 2INP NOR GATE	0000X	10102P
3110104	IC:QUAD 2INP AND GATE	0000X	10104P
3110105	IC:TRI OR GATE	0000X	10105L
3110116	IC:TRIPLE LINE RECEIVER	0000X	10116P
3110124	IC:QUAD TRANSLATOR	0000X	10124L
3110125	IC:QUAD TRANSLATOR	0000X	10125L
3110138	IC:BI-QUINARY COUNTER	0000X	10138P
3110210	IC:DUAL 3INP/3OUT OR GT	0000X	10210L
3110216	IC:TRIPLE LINE RCVR	0000X	10216L
3110231	IC:DUAL D F/F	0000X	10231L
3112000	IC:DIGITAL MIXER/TRANS	0000X	12000P
3114050	IC:NON-INVERT HEX BUFFR	0000X	14050CP
3510001	INDUCTOR: 0.1UH	72259	DD-0.10
3510003	INDUCTOR: 1.0UH	72259	DD-1.00
3510008	INDUCTOR: 0.15UH	99800	1025-00
3510010	INDUCTOR: 1.2UH	99800	1025-22
3510011	INDUCTOR: 0.12UH	72259	DD-0.12
3520007	INDUCTOR: 100 UH	99800	1537-76
4000XXX	RSTR:COMP 5% TOL. 1/8W	81349	RC05GFXXXJ
4000999	RSTR:COMP-SLECT AT TEST	81349	RC05GFXXXJ
4010XXX	RSTR:COMP 5% TOL. 1/4W	81349	RC07GFXXXJ
4010591	RSTR:COMP 5.1 OHMS 5%	81349	RC07GF5R1J
4010596	RSTR:COMP 5.6 OHMS 5%	81349	RC07GF5R6J
4010999	RSTR:COMP-SLECT AT TEST	81349	RC07GFXXXJ
4020XXX	RSTR:COMP 5% TOL. 1/2W	81349	RC20GFXXXJ
4030XXX	RSTR:COMP 5% TOL. 1W	81349	RC32GFXXXJ
4051212	RSTR:PREC 12.1K OHM 1%	81349	RN55C1212F
4053922	RSTR:PREC 39.9K OHM 1%	81349	RN55C3922F
4057500	RSTR:PREC 750 OHM 1%	81349	RN55C7500F
4061472	RSTR:PREC 14.7K OHM 1%	81349	RN55D1472F
4062261	RSTR:PREC 2.26K OHM 1%	81349	RN55D2261F
4062431	RSTR:PREC 2.43K OHM 1%	81349	RN55D2431F
4062871	RSTR:PREC 2.87K OHM 1%	81349	RN55D2871F
4064752	RSTR:PREC 47.5K OHM 1%	81349	RN55D4752F
4065621	RSTR:PREC 5.62K OHM 1%	81349	RN55D5621F
4065761	RSTR:PREC 5.76K OHM 1%	81349	RN55D5761F
4068661	RSTR:PREC 8.66K OHM 1%	81349	RN55D8661F
4101003	RSTR:PREC 100K OHM .1%	14298	AME55-C3-10038
4102003	RSTR:PREC 200K OHM.25%	14298	AME55-C3-20030
4104003	RSTR:PREC 400K OHM .5%	14298	AME55-C1-40030
4108002	RSTR:PREC 80K OHM .1%	14298	AME55-C3-80028
4110003	RSTR:WW 5 OHM 1% 7W	12436	T7(10PPM)
4110004	RSTR:WW 0.5 OHM 3% 2W	91637	RS-28
4110010	RSTR:WW 30 OHM 5% 1W	56289	239E3005
4110012	RSTR:WW 0.66 OHM 3% 4W	91637	RS-2
4110013	RSTR:WW 0.15 OHM 3% 5W	91637	RS-5
4120008	RSTR:CBN FLM 8.2 OHM 5%	0000L	R25-8.2-5%-1/4W
4120010	RSTR:CMT FLM 1.00MEG 1%	01121	CC1004F
4120011	RSTR:CMT FLM 2.00MEG 1%	01121	CC2004F
4120012	RSTR:CMT FLM 4.02MEG 1%	01121	CC4024F
4130XXX	RSTR:MET OX-100PPM-1/4W	24546	C4/2%/OHMS
4130999	RSTR:MTOX-SLECT AT TEST	24546	C4/2%/XXX
	NOTE: 498P- RESISTORS NON-INDUCTIVE WIREWOUND		
4140030	RSTR:PREC 9K OHM .01%	05591	TYPE 498P1S8
4140031	RSTR:PREC 10K OHM .01%	05591	TYPE 498P1S8
4140032	RSTR:PREC 20K OHM.025%	05591	TYPE 498P1S8
4140033	RSTR:PREC 40K OHM .05%	05591	TYPE 498P1S8
4140034	RSTR:PREC 3K OHM .1%	05591	TYPE 498P1S8
4140035	RSTR:PREC 8K OHM .1%	05591	TYPE 498P1S8
4140039	RSTR:PREC 3.7K OHM .1%	05591	TYPE 498P1S8
4170001	RSTR NETWORK:15X15K 2%	80740	898-1-R15K
4250003	RSTR:VAR CER 1K OHM	73138	72XWR1K
4250006	RSTR:VAR CER 10K OHM	73138	72XWR10K
4250008	RSTR:VAR CER 100K OHM	73138	72XWR100K
4250009	RSTR:VAR CER 500 OHM	73138	72XWR500
4250011	RSTR:VAR CER 10 OHM	73138	72XWR10
4280009	RSTR:VAR WW 500 OHM	73138	89PR-500
4290001	RSTR:VAR 250K/SPDT SW	11236	EF8078/RVF45
4500008	SWITCH:P/B (PWR IND)	EIP	SRCE CONT DWG
4500010	SWITCH:P/B,8-STATN(451)	EIP	SRCE CONT DWG
4510001	SWITCH:TOG,SPDT,120V,5A	09353	7101H
4510007	SWITCH:TOG,DPDT,125V,3A	04009	8305SQ
4540002	SWITCH,THUMBWHEEL: BCD	23880	900048
4540003	SWITCH:PC 7CKT,SPST	23880	1007-692
4703563	XSTR: NPN	07263	2N3563

TABLE 8-3 (Continued). MASTER PARTS LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
4704124	XSTR: NPN GP	04713	2N4124
4704126	XSTR: PNP GP	04713	2N4126
4704401	XSTR: NPN	04713	2N4401
4704416	XSTR: N-CHAN JFET	04713	2N4416
4704959	XSTR: PNP RF	04713	2N4959
4705983	XSTR: NPN PWR	04713	2N5983
4705989	XSTR: NPN PWR	04713	2N5989
4710002	XSTR: PNP PWR	04713	MJE370
4710003	XSTR: NPN PWR	04713	MJE520
4710009	XSTR: PNP	04713	MJE350
4710010	XSTR: PNP RF	04713	MPS-H81
4710011	XSTR:GRADED 2N5179-RED	EIP	4705179
4710012	XSTR:GRADED 2N5179-YEL	EIP	4705179
4710013	XSTR:GRADED 2N5179-GRN	EIP	4705179
4710015	XSTR:MTCH PR,2N5179-YEL	EIP	4710012
4710017	XSTR:NPN RF SW	04713	MMT3960
4710018	XSTR: PNP AMPL	04713	MPS-L51
4710019	XSTR: PNP AMPL	04713	MPS-D55
4710021	XSTR: NPN AMPL	04713	MPS-D05
4710022	XSTR: N-CHAN JFET	01295	TIS73
4710023	XSTR: PNP RF	01295	A5T4261
4710024	XSTR: NPN RF	73445	BFR90
4720002	XSTR: NPN RF	04713	2N3866(MOT)
4900004	TRANSFORMER,POWER	EIP	SPEC.CONT.DWG
5000012	FAN,AXIAL,115VAC	23936	8500
5000055	TILT RAIL	21793	453458
5000058	KNOB:RND W/INSERT .51D	86797	R867-0ML.25SHFT
5000060	KEY,POLARIZING,PCB CONN	04618	530030-1
5000079	FUSE: .750A,SB,3AG,250V	71400	MDL-3/4A
5000101	FUSE: 1.5A,SB,3AG,250V	71400	MDX-1-1/2
5000112	BATTERY CLIP, 1/2"SPCG	83330	1234
5210023	COVER,ENCL: TOP	21793	453453
5210024	COVER,ENCL: BOTTOM	21793	453454
5220003	FOOT,PLASTIC:ENCLOSURE	21793	453457
5280016	CONN:MODIFIED, 24 PIN	EIP	M/F:2640024
5440002	LINE CORD SET, 3-COND	70903	17250

ADDITIONAL ENTRIES TO PRECEDING LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
2150008	CAP: CER .005 UF 20% 100V	56289	TG-D50
2350018	CAP: FDTH: RF FLTR, 5,000 PF	72982	1270-016
2350021	CAP: TRIM 2-8 PF, 250V	0000B	10S-T-24-2/8
2630009	SOCKET: 14 PIN IC	71785*	14-N-DIP
2630010	SOCKET: 16 PIN IC	71785*	16-N-DIP
2560028	CONN: RCPT, KEYED, 6 PIN, M/F	0000M	RG1.B.306.C
3084123	IC: TTL/MONOSTABLE MV	0000X	74LS123N
3084155	IC: DUAL 2/4 LINE DECODER	0000X	74LS155N
3084193	IC: UP/DN BINARY COUNTER	0000X	74LS196N
3084196	IC: PST DECADE COUNTER	0000X	74LS4196
3084257	IC: 2:1 MUX	0000X	74LS257N
3084393	IC: DUAL 4-BIT BINARY CNTR	0000X	74LS393P
3084490	IC: DUAL 4-BIT DECADE CNTR	0000X	74LS490P
3087400	IC: QUAD 2-INPUT NAND GATE	0000X	74LS00N
3087402	IC: QUAD 2-INPUT NOR GATE	0000X	74LS02N
3087404	IC: HEX INVERTER	0000X	74LS04N
3087405	IC: HEX INVERTER	0000X	74LS05N
3087408	IC: QUAD 2-INPUT AND GATE	0000X	74LS08N
3087413	IC: DUAL 4-INPUT NAND TRIGGER	0000X	74LS13N
3087420	IC: DUAL 4-INPUT NAND GATE	0000X	74LS20N
3087430	IC: 8-INPUT NAND GATE	0000X	74LS30N
3087432	IC: QUAD 2-INPUT OR GATE	0000X	74LS32N
3087447	IC: BCD/7-SEGMENT DECODER	0000X	74LS47N
3087475	IC: QUAD LATCH	0000X	74LS75N
3087476	IC: DUAL J-K F/F	0000X	74LS76N
3087486	IC: QUAD 2-INPUT EXCL OR GATE	0000X	74LS86N
3087490	IC: DECADE COUNTER	0000X	74LS90N
3087493	IC: 4-BIT BINARY COUNTER	0000X	74LS93N
4710001	XSTR: NPN PWR	0000X	MJE3055
4710026	XSTR: NPN RF	0000X	NE73432B

* CINCH DIV., TRW CORP., ELK GROVE VILLAGE, IL 60007

TABLE 8-3 (Continued). MASTER PARTS LIST

SECTION 9

CIRCUIT SCHEMATICS & DESCRIPTIONS

COMPONENT LOCATORS

9-1. GENERAL

9-2. Schematics and Component Locators are arranged by Assembly number (A101, A102, etc.). Circuit descriptions and circuit theory are shown on the same or adjacent pages. All assembly related drawings and diagrams have the same figure number, but have different suffix letters (9-6A, 9-6B, etc.).

9-3. Parts Lists and Ordering Information will be found in Section 8.

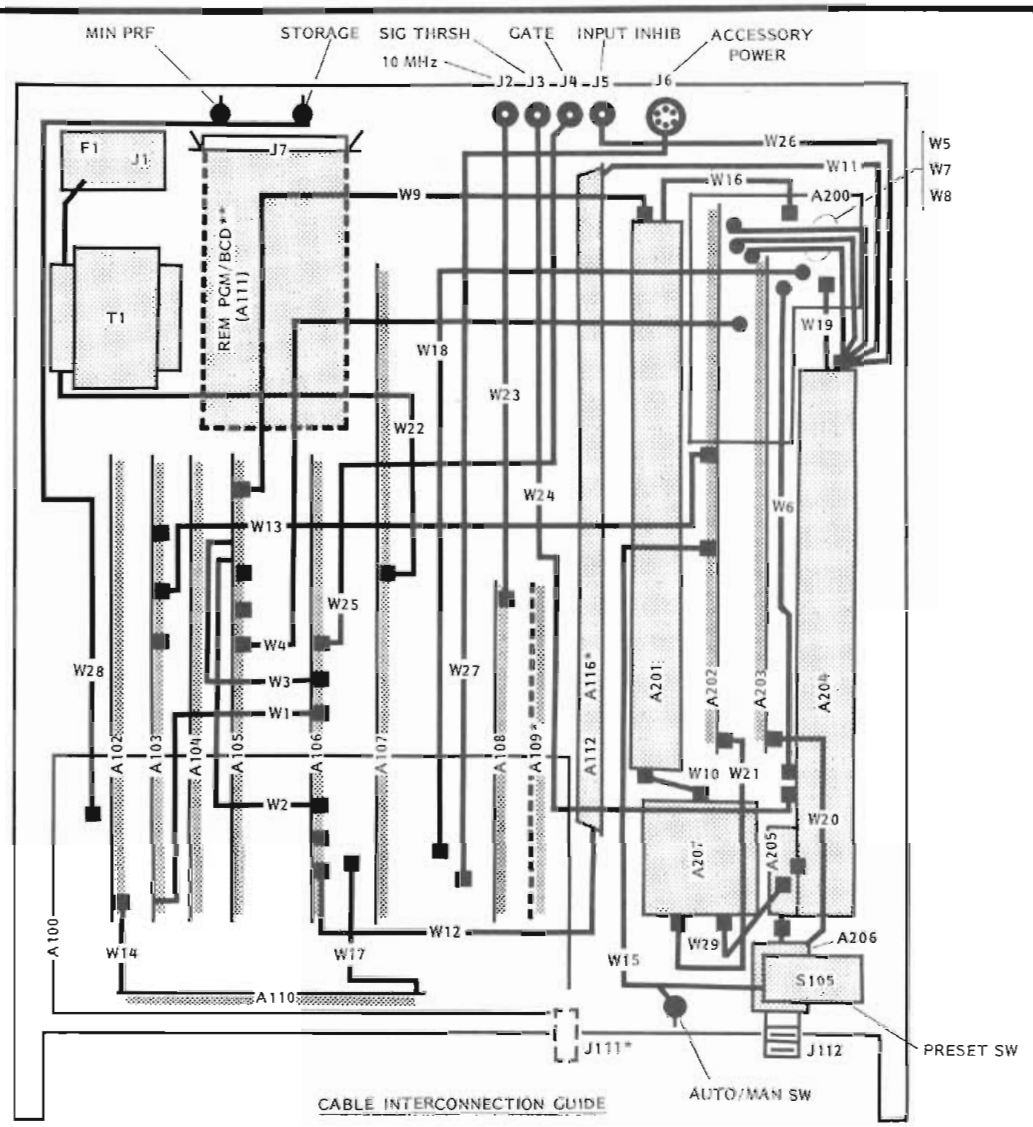
9-4. Unless otherwise specified, the following notes apply to all figures in this section.

a. Resistance values in ohms.

b. Capacitance values in microfarads ("pf" values in picofarads).

c. Connector reference numbers may not appear on part.

d. SAT = Selected at Test. Nominal value shown; part may not be installed. MP = Matched Pair.



CABLE INTERCONNECTION GUIDE

FROM	CABLE	TO
A103-P2	W1	A106-J5
A105-P2	W2	A106-J1
A105-P3	W3	A106-J4
A200-P2	W4	A105-J1
A200-P3	W5	A204-J6
A200-P4	W6	A204-J2
A200-P5	W7	A204-J7
A200-P6	W8	A204-J4
A201-J1	W9	A105-J4
A201-J2	W10	A207-J2
A112-P1	W11	A204-J3
A112-P2	W12	A106-J3
A103-J3	W13	A202-J2
A110-P2	W14	A102-J1
A1-P121	W15	A202-J1**
A201-P1	W16	A200-J2
A110-P1	W17	A100-J2
A200-P1	W18	A100-J3
A204-P1	W19	A200-J1

FROM	CABLE	TO
A206-P2	W20	A203-J1
A202-J1	W21	A1-Q1
		A107-J3
A1(T1)P101	W22	A107-J1
A1(J2)P102	W23	A108-J1
A1(J3)P103	W24	A204-J1*
A1(J4)P104	W25	A106-J6
A1(J5)P105	W26	A204-J5*
A1(J6)P106	W27	A100-J8
A1-P107	W28	A100-J1
A205-P1	W29	A207-J1

*PRESCALER OPT. P2 A109, A116)

FROM	CABLE	TO
A1-P103	W24	A109-J6
A1-P105	W26	A109-J3
A1-J111	W30	A109-J1
A204-J1	W31	A109-J5
A204-J5	W32	A109-J4
A105-J2	W33	A109-P2
A116-P1	W34	A109-J2
A116-P2	W35	A106-J2

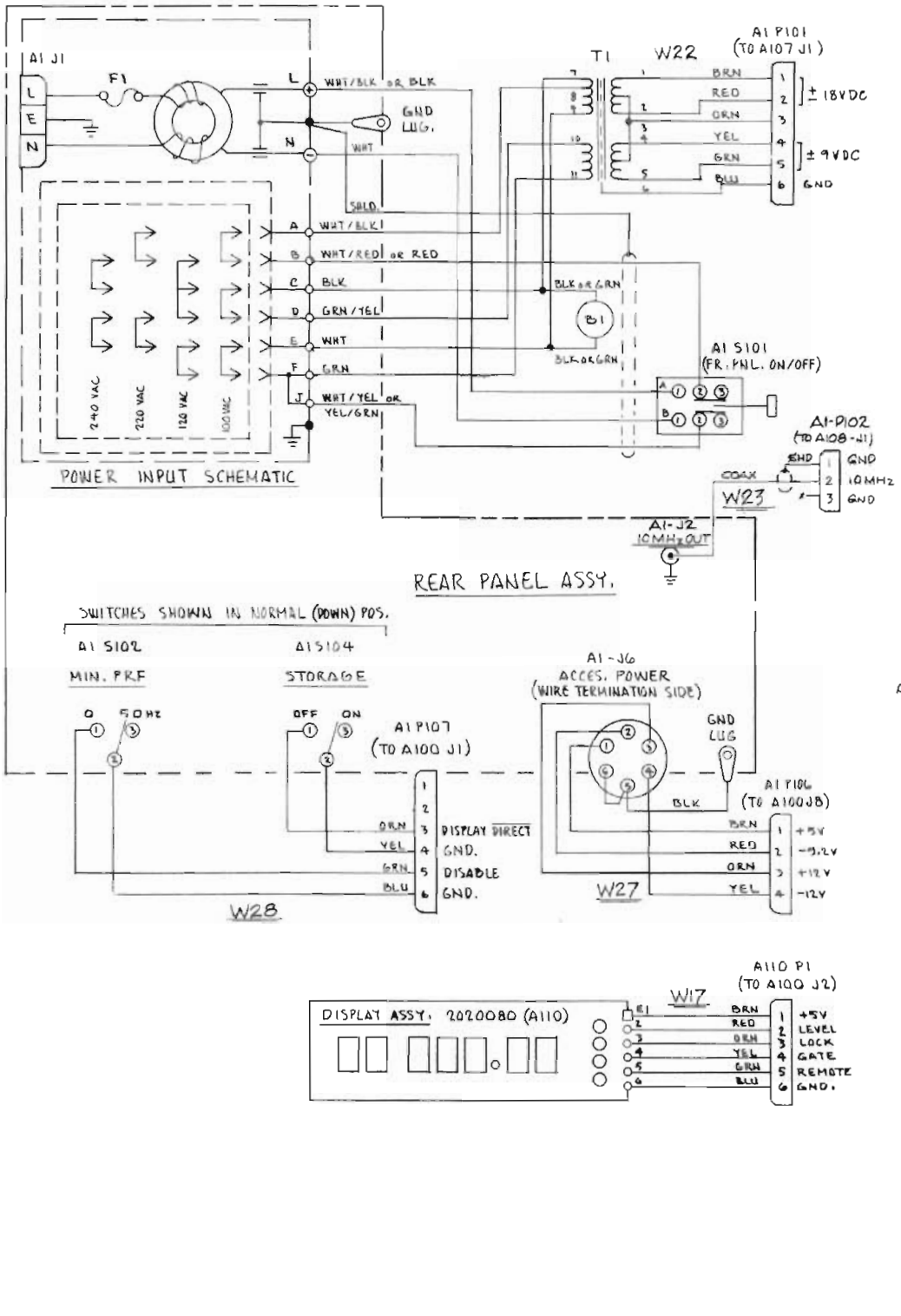
**REM PGM/BCD OUT OPT. P4 (A111)

FROM	CABLE	TO
A1-P121	W15	A100-J6
A111-J1	W40	A100-J4
A111-J2	W41	A100-J5
A111-J3	W41	A100-J6
A111-J4	W42	A202-J1
A111-J5	W43	A103-J5
A111-J6	W44	A103-J1

DANA EIP

451

FIGURE 9-1
ASSEMBLY LOCATOR
CABLE INTERCONNECTIONS


A1 J1
L
E
N
F1
WHT/BLK OR BLK
GND LUG.
WHT
SOLD
A WHT/BLK
B WHT/RED OR RED
C BLK
D GRN/YEL
E WHT
F GRN
J WHT/YEL OR YEL/GRN
240 VAC
220 VAC
120 VAC
100 VAC
POWER INPUT SCHEMATIC
T1
W22
A1 P101
(TO A107 J1)
BRN
RED
ORN
YEL
GRN
BLU
± 18VDC
± 9VDC
GND
BLK OR GRN
B1
A1 S101
(FR. PNL. ON/OFF)
A1-P102
(TO A108-J1)
SHD
COAX
GND
10MHz
GND
W23
A1-J2
10MHz OUT
REAR PANEL ASSY.
SWITCHES SHOWN IN NORMAL (DOWN) POS.
A1 S102
MIN. PRF
0
50Hz
A1 S104
STORAGE
OFF
ON
A1 P107
(TO A100 J1)
ORN
YEL
GRN
BLU
DISPLAY DIRECT
GND.
DISABLE
GND.
W28
A1-J6
ACCES. POWER
(WIRE TERMINATION SIDE)
GND LUG
BLK
A1 P106
(TO A100J8)
BRN +5V
RED -5.2V
ORN +12V
YEL -12V
W27
A110 P1
(TO A100 J2)
W17
DISPLAY ASSY. 2020080 (A110)
BRN +5V
RED LEVEL
ORN LOCK
YEL GATE
GRN REMOTE
BLU GND.
(A200)
CONVERTER INTERCONN. ASSY.
2020090
(A201)
SOURCE / AMPLIFIER ASSY.
2010091
(A204)
IF PROCESSOR ASSY.
2010094
HARNESS ASSY
TO A207J3
A1Q1
HARNESS
(A206)
LIMITER/ ATTN. ASSY.
2010096

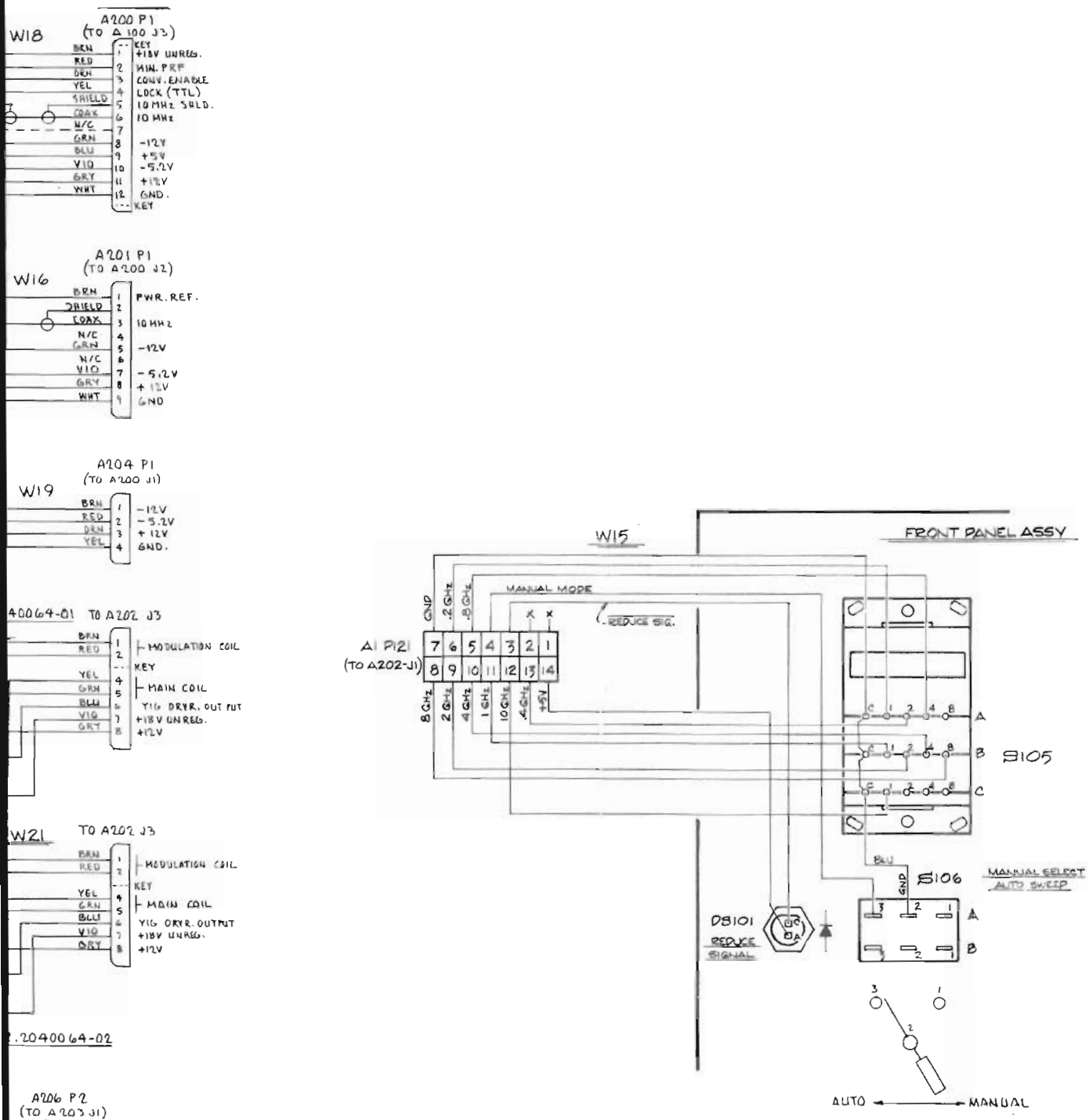
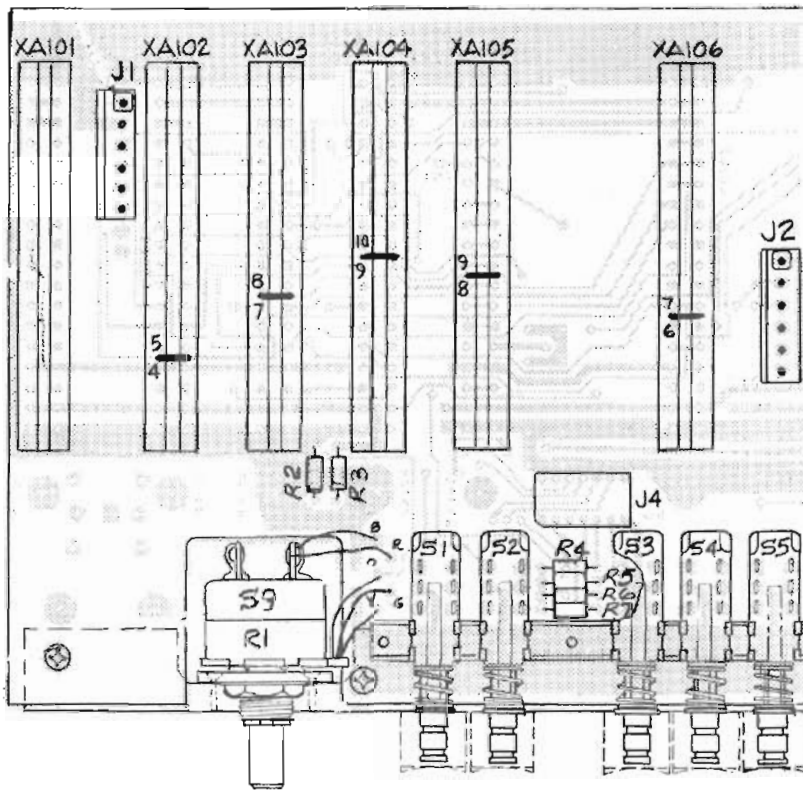
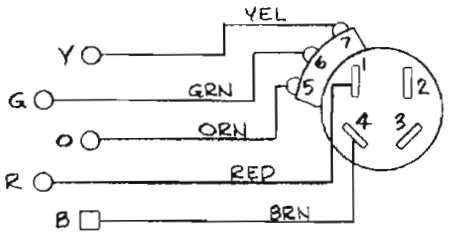


FIGURE 9-2
INTERCONNECTION
DIAGRAM


XA101
XA102
XA103
XA104
XA105
XA106
J1
J2
J4
S1
S2
S3
S4
S5
R1
R2
R3
R4
R5
R6
R7
5
4
8
7
10
9
9
8
7
6


YEL
Y
GRN
G
ORN
O
RED
R
BRN
B
7
6
5
1
2
4
3

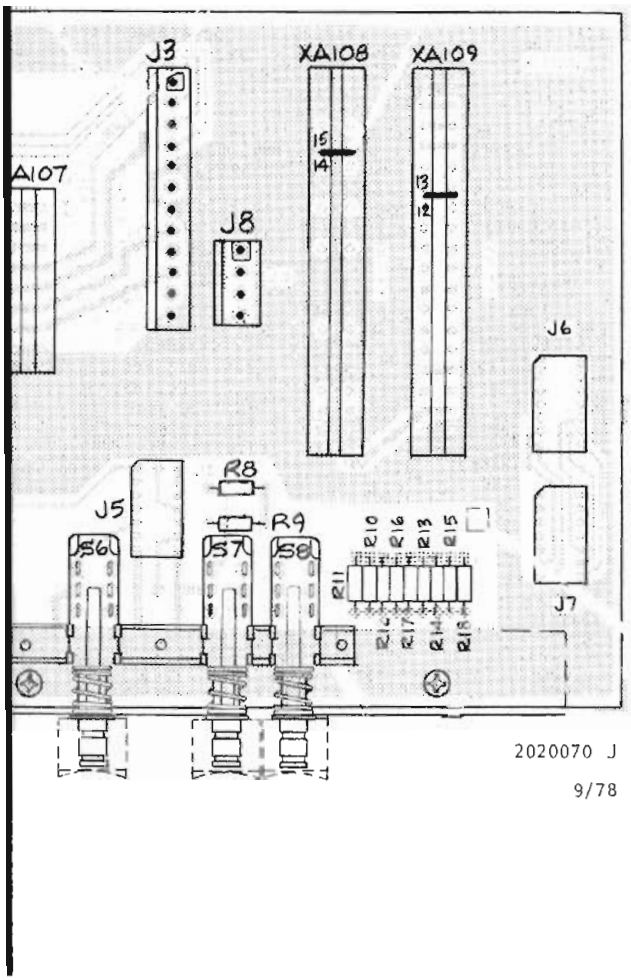
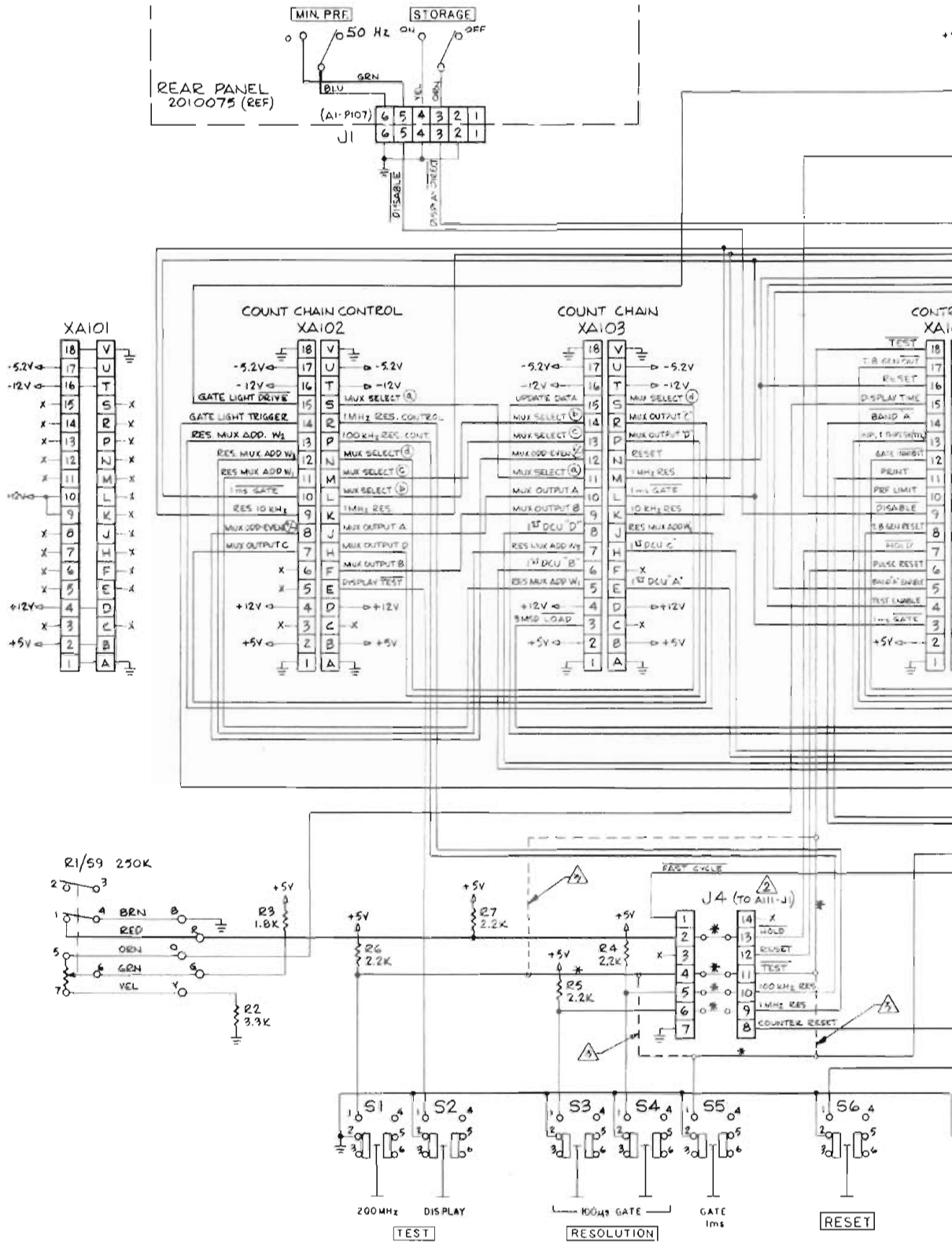
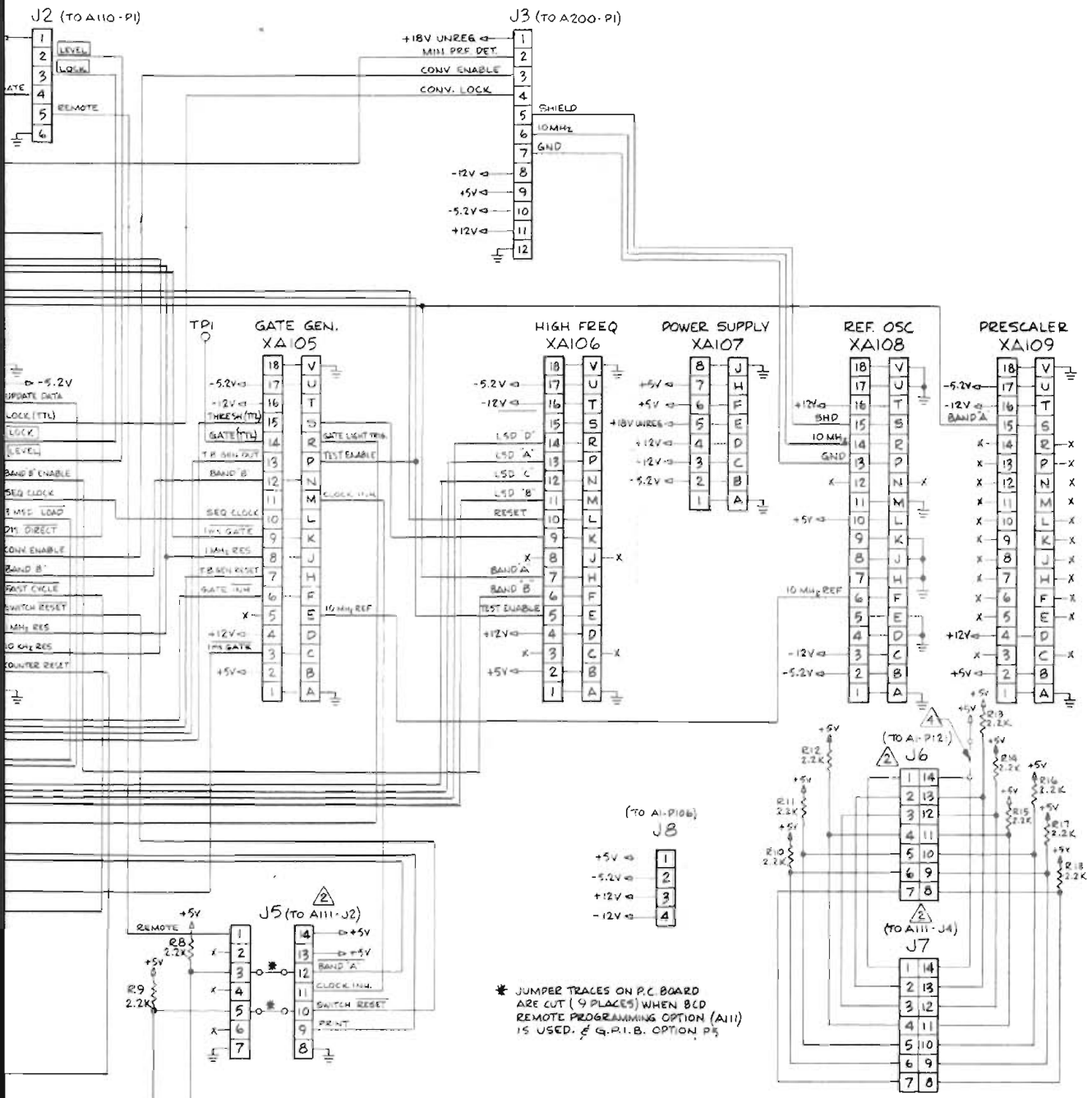


FIGURE 9-3A
COMPONENT LOCATOR
COUNTER INTERCONNECT (A100)


MIN. PRF.
STORAGE
50 Hz
ON
OFF
GRN
BLU
YEL
ORN
REAR PANEL
2010075 (REF)
(A1-P107)
J1
DISABLE
DISPLAY TRIGGER
XA101
COUNT CHAIN CONTROL
XA102
COUNT CHAIN
XA103
-5.2V
-12V
+12V
+5V
GATE LIGHT DRIVE
GATE LIGHT TRIGGER
RES. MUX ADD. W3
RES MUX ADD W2
RES MUX ADD W1
1ms GATE
RES 10 KHz
MUX ODD-EVEN
MUX OUTPUT C
MUX SELECT d
MUX SELECT c
MUX SELECT b
1MHz RES.
MUX OUTPUT A
MUX OUTPUT B
DISPLAY TEST
100 KHz RES. CONT.
UPDATE DATA
MUX SELECT a
MUX OUTPUT D
RESET
10 KHz RES
SHIFT LOAD
DCU "D"
DCU "C"
DCU "B"
DCU "A"
R1/S9 250K
R3 1.8K
R7 2.2K
R6 2.2K
R4 2.2K
R5 2.2K
R2 3.3K
BRN
RED
ORN
GRN
YEL
FAST CYCLE
J4 (TO A111-J)
HOLD
RESET
TEST
100 KHz RES
1 MHz RES
COUNTER RESET
S1
S2
S3
S4
S5
S6
200 MHz
DISPLAY
TEST
100 KHz GATE
RESOLUTION
GATE
1ms
RESET



(TO A1-P106)

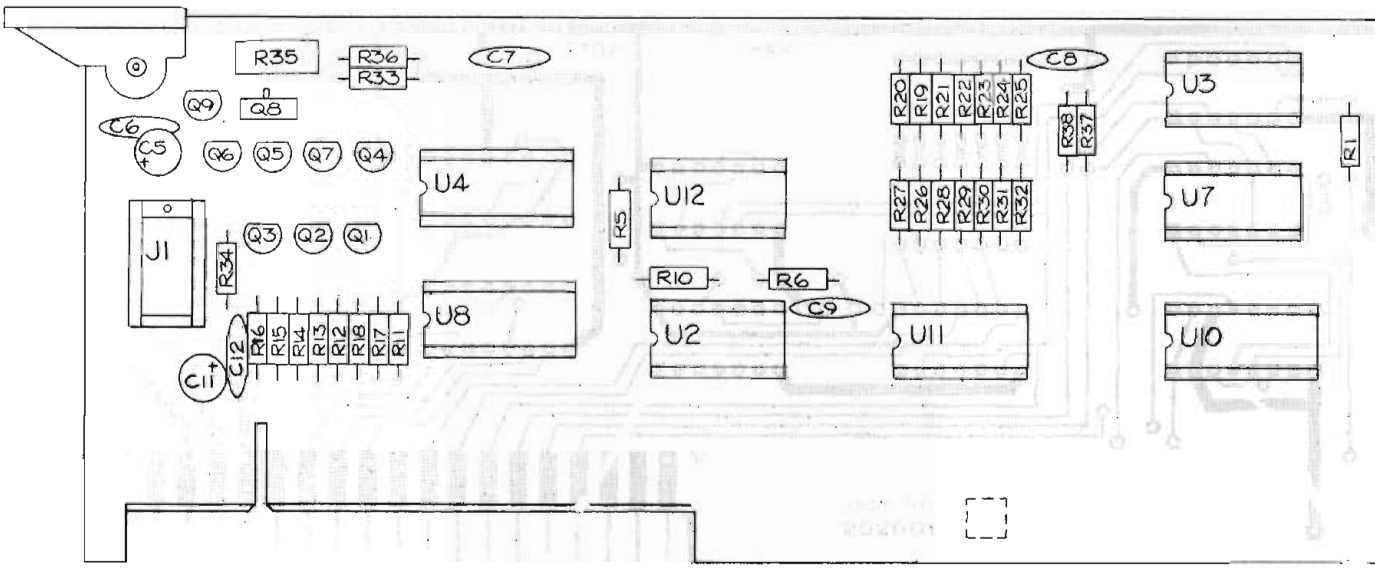
(TO A1-P12)

(TO A111-J4)

* JUMPER TRACES ON P.C. BOARD ARE CUT (9 PLACES) WHEN BCD REMOTE PROGRAMMING OPTION (A111) IS USED. & G.P.I.B. OPTION P5

5500070 D
July 1979

FIGURE 9-3B
SCHEMATIC DIAGRAM
COUNTER INTERCONNECT (A100)



COUNT CHAIN CONTROL (A102)

General

Count Chain Control A102 controls and processes the flow of information on Count Chain board A103, and drives the front panel visual display. A pulse-stretcher and driver (on A102) also operate the GATE indicator on the front panel of the counter.

The clock generator, a ÷16 counter, and a 3-8 line decoder, serve to produce a sequence of eight addresses. These cause the DCU's on A103 to read out their BCD contents, in sequence, back to the data input of A102. The digits of the number representing the frequency measured by the counter are thus read in sequence into A102. The BCD numbers are decoded by U8 to drive the segments of each display digit on Display board A110. The same address generator that selected DCU's on A103, now addresses and drives the proper display digit of A110, so the number of a particular DCU of A103 will be displayed in the proper position. The address drive to certain display digits may be removed (to blank these digits) via the RESOLUTION switches.

The gate trigger is applied to a pulse-stretcher on A102. This insures that the gate control signal is of sufficient duration that the GATE indicator will produce a visible flash for each measurement cycle of the counter. (Short gates of 100 µs would not otherwise be visible.)

Display Address Generator (U8, U9-11)

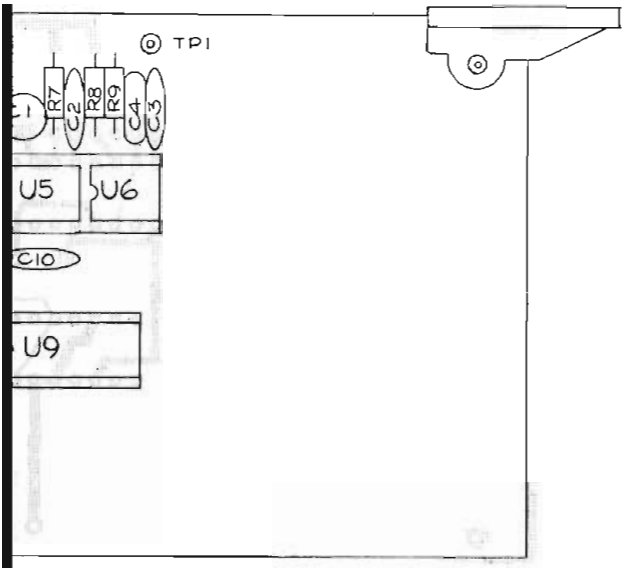
The Address Generator is driven by the clock generated in U6 at a 200 kHz rate. This drives binary counter U9, producing a sequence of sixteen different states on its four output lines. The last three lines: B, C, and D, drive decoder U10 which produces an output on one of eight output lines for each of the eight different states of the inputs: B, C, and D.

Seven of the eight single line outputs of decoder U10 are used to select display digits directly. The address to the DCU's of A103 however, is a one-of-four line code, plus an odd-even code on a fifth line. The one-of-four line code is obtained by combining successive outputs of decoder U10 in groups of two in the four AND gates of U11. The odd-even code is simply the A input to U10.

Display Decoder, Driver, and Leading Zero Suppression Circuits (U2, U4, U8)

The BCD to 7-segment decoder is included in U8. It directly supplies the cathode currents to the segments of the display digits which must be illuminated to display the number given by the BCD code. Additional inputs to U8 allow all outputs to be activated simultaneously (Lamp Test which displays all 8's), all outputs turned off simultaneously (BI/RBO which blanks the display), or the output blanked if the BCD input is zero (RBI). This last input is used in leading zero suppression.

The anode currents of the seven display digits are supplied by the seven individual digit drivers Q1-Q7. These drivers are turned on in sequence by outputs 1 through 7 of U10, and effectively apply the +5 volt adjustable supply to the anodes of the display digits. The segment currents are then determined by the segment drive outputs of U8, and the seven resistors in the output lines. (Active outputs are driven to ground so output currents will be determined by the value of the series resistors.) Corresponding segments of all display digits are wired in parallel, with all seven display digits being driven simultaneously by the 7-line decoder. Only one of these digits is supplied anode current by the digit drivers at any given time. The correct BCD input to U8 is selected by address decoders on the Count Chain (A103).



2020084 F
9/78

The zero suppression circuits cause all digits to the left of the first non-zero display to be blanked. Outputs of decoder U10 are processed in U2, U4, U8, and U12, to produce this result.

Decoder outputs of U10 occur in regular time sequence 0 through 7. Defining the interval in which output 0 is active as TF0 (Time Frame 0), then intervals TF0, TF1 ..... TF7, are of equal length, and occur in a regular repetitive sequence. Display digits are driven in Time Frames TF1 - TF7. The zero suppression latches are reset in TF0 of each sequence. The BCD output from A103 is coded to be always zero in TF0. This is decoded in data detector U2 to produce a high at the set input to the U4B latch. U9A output, and U10 TF0 output, are combined in U3 and U7 to produce a reset input to U4B at TF½ (the second half of TF0). U4B is then always reset at the beginning of the TF1-TF7 sequence. During this sequence, the DCU outputs of A103 are addressed and read out in sequence: 10 GHz, 1 GHz ... 100 kHz. If any of these BCD outputs are non-zero, detector U2 immediately sets U4B. U4B is then reset until the left-most non-zero digit of the display appears after which it remains set through the remainder of each display sequence. This flip-flop is used to remove the suppression when all digits are zero, otherwise the display would disappear completely if there were no input to the counter (zero frequency). The narrow MUX clock is applied to the non-zero data detector via U12 to disable the detector during clock pulses, so switching transients do not cause problems.

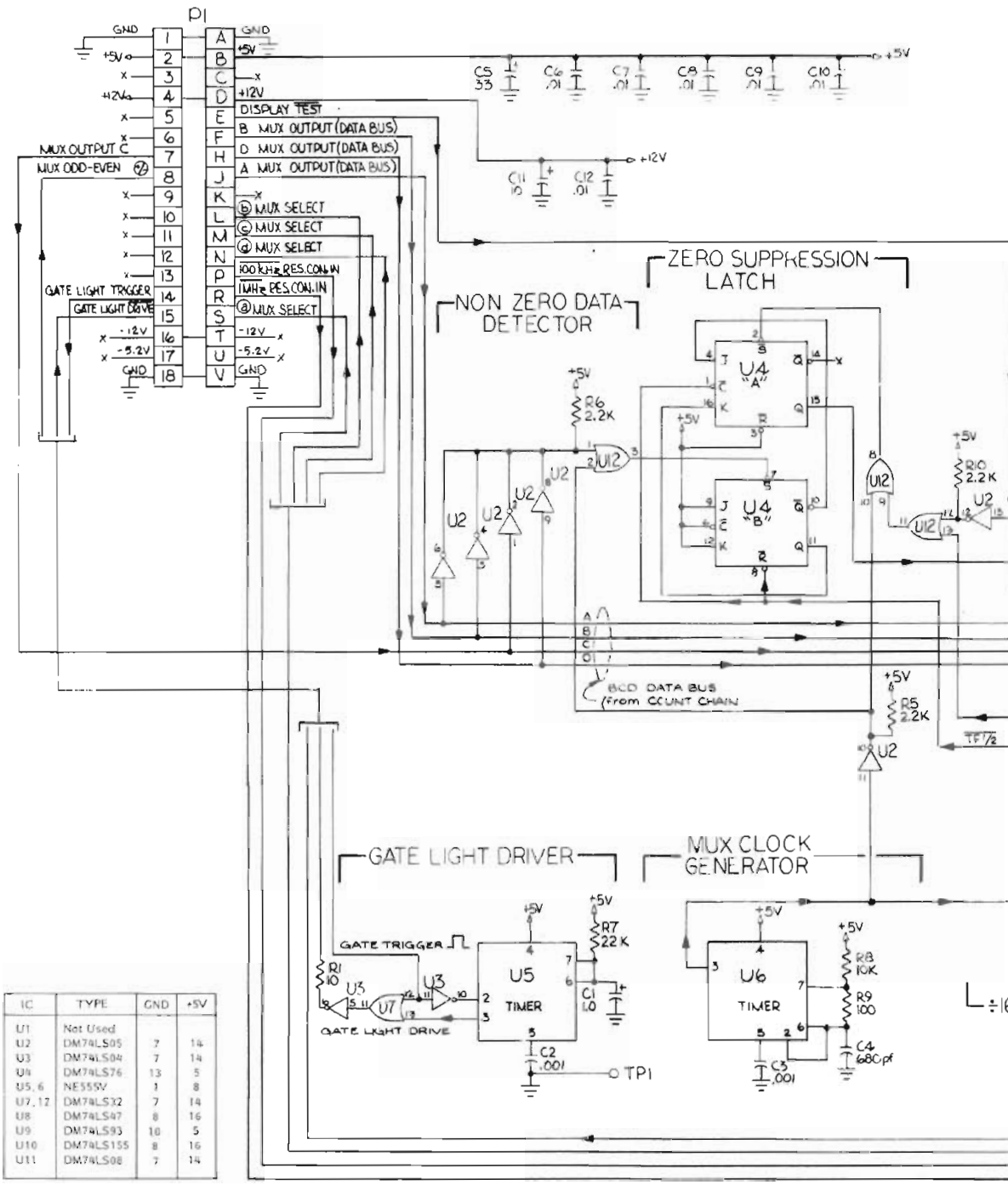
Flip-flop U4A controls the zero suppression directly. If U4B is in the set state at the end of a display sequence, then U4A is reset by the clock pulse at TF½ of the next sequence. If U4B is in the reset state at the end of TF7, then U4A is set at TF½ of the next sequence. If non-zero data occurs in a display sequence, U4A is set and enables zero suppression in the next sequence. If all data is zero through a sequence, U4A is set and disables zero suppression in the next sequence. Assuming that many display sequences occur for each set of BCD data, then all zero data receives no suppression, and all zeros are displayed, while non-zero data has leading zeros suppressed.

U4A enables zero suppression in its reset state by applying the low Q output to the ripple blanking RBI input of U8. With this input low, all decoder outputs are shut off when the data is low and the BI/RBO output is also low. When ever data becomes non-zero, BI/RBO goes high and sets U4A, removing the RBI input enable. This can only be again enabled at the start of a following sequence when U4A may be reset.

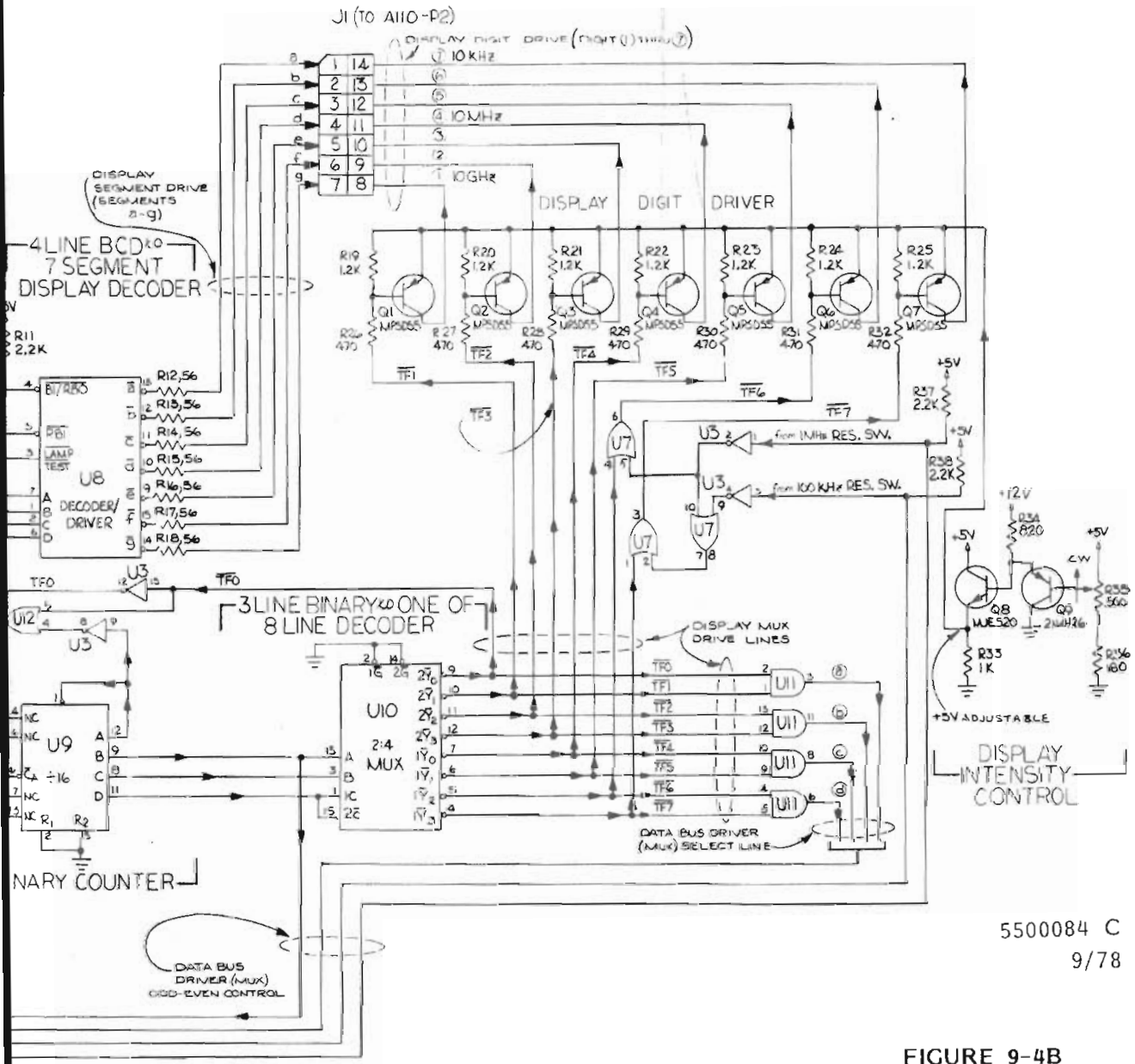
Gate Indicator Driver (U3, U5, U7)

The front panel GATE indicator is driven directly by OR gate U7C in response to the gate trigger from A105. A second input to this gate is obtained from U5 which is also set by the gate trigger via inverter U3E. U5 is a one-shot whose period is set to about 30 ms. The drive pulse to the indicator in response to each gate trigger is then of sufficient duration to be visible, even for very short gate times.

FIGURE 9-4A
COMPONENT LOCATOR
COUNT CHAIN CONTROL (A102)

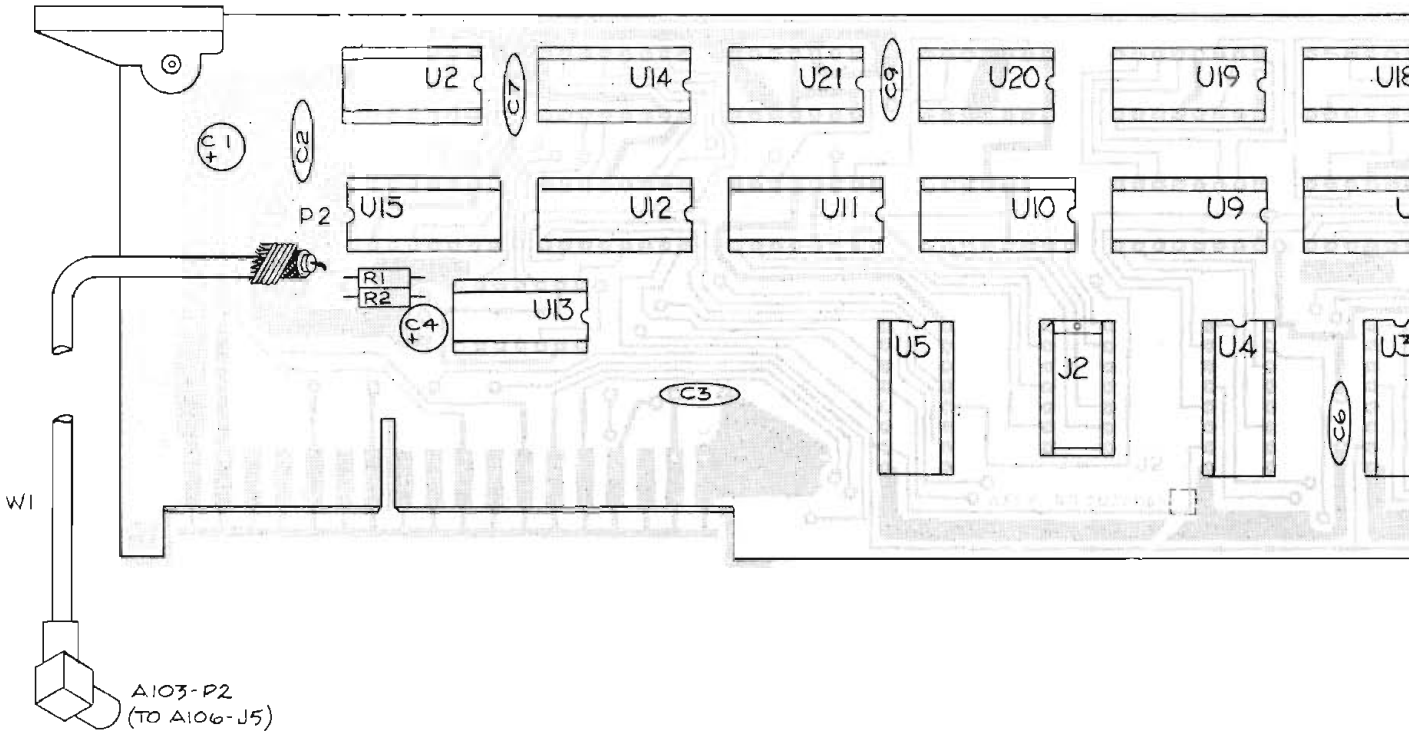


IC	TYPE	GND	+5V
U1	Not Used		
U2	DM74LS05	7	14
U3	DM74LS04	7	14
U4	DM74LS76	13	5
U5, 6	NE555V	1	8
U7, 12	DM74LS32	7	14
U8	DM74LS47	8	16
U9	DM74LS93	10	5
U10	DM74LS155	8	16
U11	DM74LS08	7	14



5500084 C
9/78

FIGURE 9-4B
SCHEMATIC DIAGRAM
COUNT CHAIN CONTROL (A102)



COUNT CHAIN (A103)

General

Count Chain board A103 accumulates the counts provided by the output of High Frequency board A106, and on command, stores this BCD information in a separate storage unit. A multiplexer scans the information one digit at a time, and presents the BCD digits serially on a four line output bus. (For Option P4, the same information is presented in parallel form to the rear panel BCD Output connector.) The last three DCU's of the counting chain may be preset before normal counting begins.

The 451 Counter measures frequencies by dividing the input frequency in cascaded Decimal Counting Units (DCU's) for a precisely determined gate time. The number of accumulated counts, divided by the gate time, gives the frequency directly. The first DCU is on A106, and is followed by seven additional DCU's on this board. Each DCU has a four-line BCD output to show its accumulated count. These BCD outputs are decoded and drive the front panel display which shows the value of the digits accumulated by each of these DCU's.

Counting Chain (U16-21)

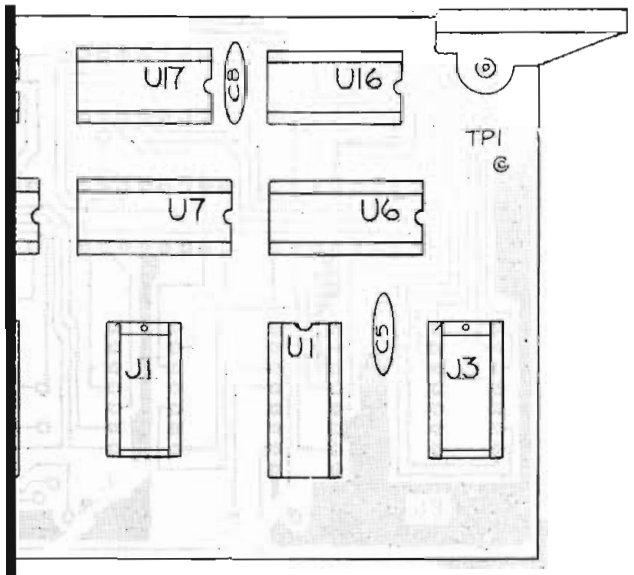
The counting chain incorporates seven DCU's. The first two are higher speed than the remaining five, as they must operate at higher frequencies. Except for the first DCU, the D output of each DCU directly drives the clock input of the next DCU. The first DCU is presettable by the 1 ms gate command. When this command is not activated, the DCU is held in the "9" state. The DCU carry from the High Frequency board (A106) then bypasses the first DCU and directly clocks the second DCU. When the 1 ms gate command is activated, the preset is removed, and the DCU carry clocks the first DCU which clocks the second. In this state, the first DCU is effectively placed in the count chain. The last three DCU's may be preset to any desired number by applying a load command before normal counting begins. This is used to add the Converter local oscillator frequency to the counting chain to obtain the actual input frequency in Band B.

Storage Unit (U6-12, U14)

Seven 4-bit latches are provided which store the information from the DCU's. The last six are driven directly from the BCD information of each corresponding DCU. The first one is driven from a data selector multiplexer which is controlled by the 1 ms gate command. When this command is not activated, the data selector presents the BCD information from A106 to the latch. When the 1 ms gate command is activated, the data selector selects the BCD information from the first DCU on this board.

Storage Unit (U6-12, U14)

Seven 4-bit latches are provided which store the information from the DCU's. The last six are driven directly from the BCD information of each corresponding DCU. The first one is driven from a data selector multiplexer



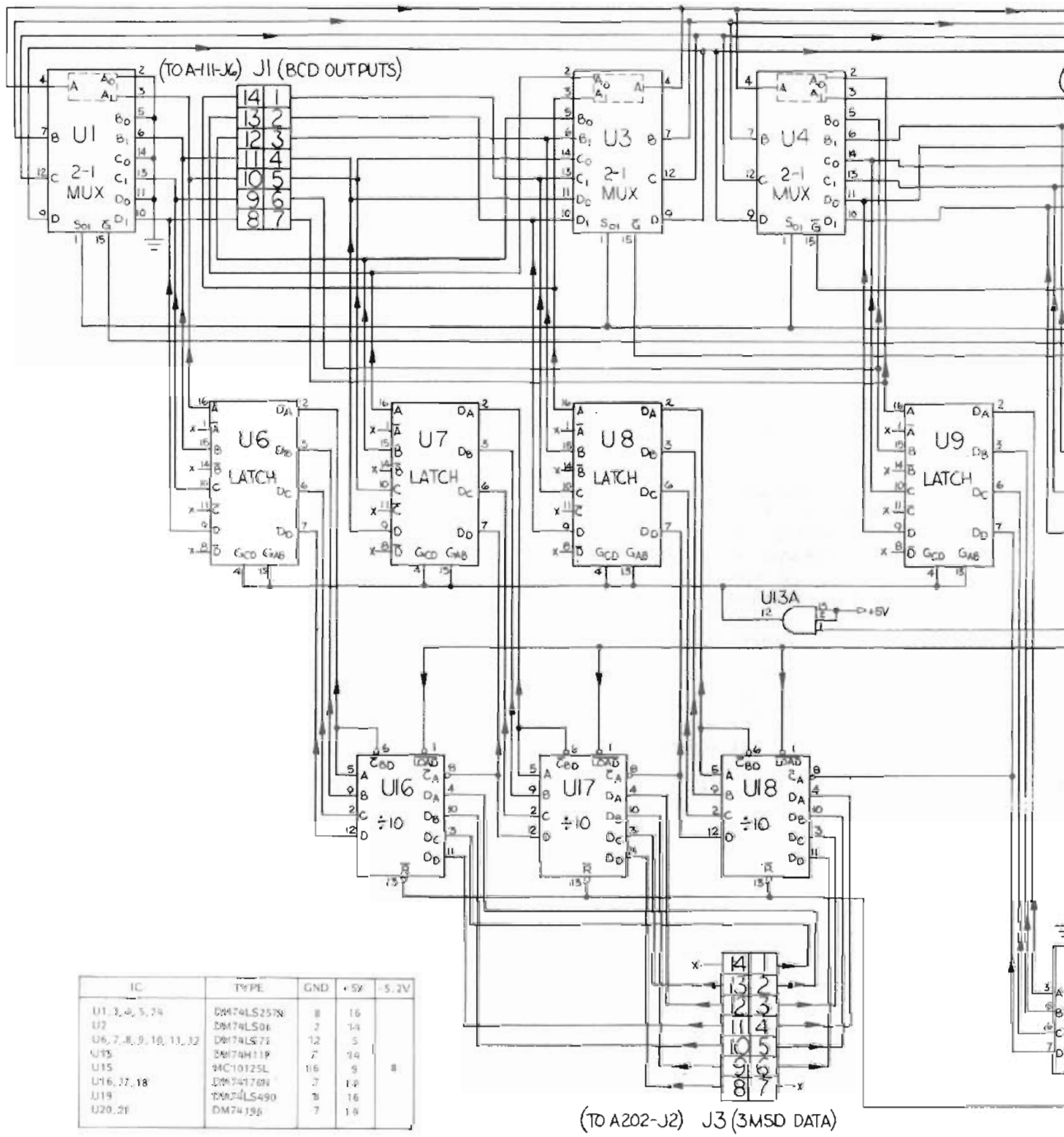
2020083 D
9/78

which is controlled by the 1 ms gate command. When this command is not activated, the data selector presents the BCD information from A106 to the latch. When the 1 ms gate command is activated, the data selector selects the BCD information from the first DCU on this board. A load command to all latches, causes the DCU information to be stored and held until the next load command. All information from the counting chain to the balance of the counter, is obtained from these latches.

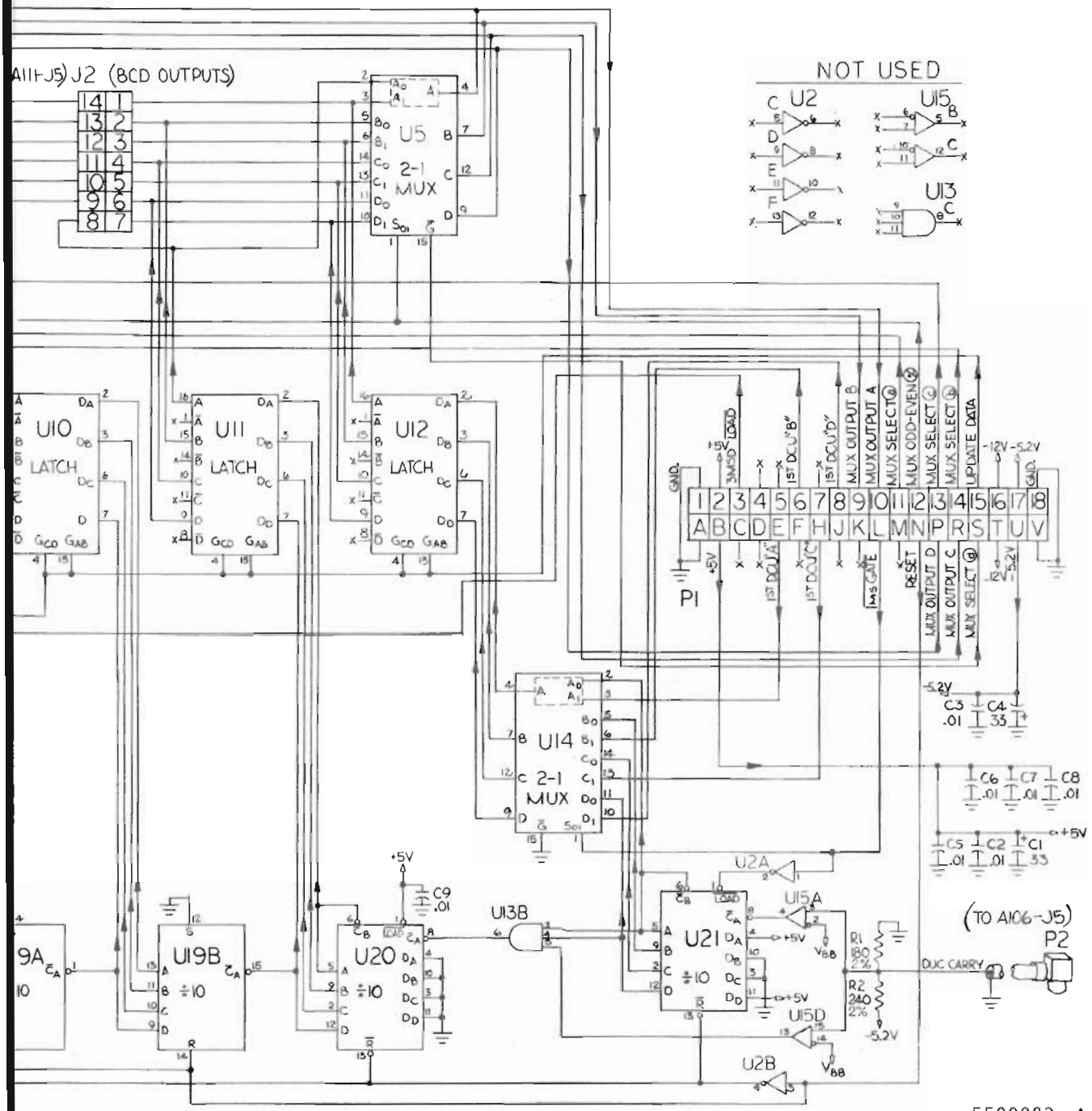
Data Output Multiplexer (U1, U3-5)

The multiplexer converts the parallel BCD information located in the latches, to the serial form necessary to drive the front panel display. Each multiplexer has tri-state outputs — this means that the multiplexer can be gated into an active or passive state. In the passive state, the output is a high impedance which does not respond to the input, thereby allowing the output to be controlled by another IC. Each IC contains four separate channels, with one output and two inputs per channel. A select input to each IC allows one or the other of the inputs to be transferred to the output. The parallel BCD information from the latches is directly applied to the multiplexer inputs. An input select line (MUX Odd/Even), combined with a four-line gating bus (MUX Select Bus), serially selects this BCD information and places it on the multiplexer outputs which are tied together. The end result is serial BCD information which corresponds to the input frequency.

FIGURE 9-5A
COMPONENT LOCATOR
COUNT CHAIN (A103)

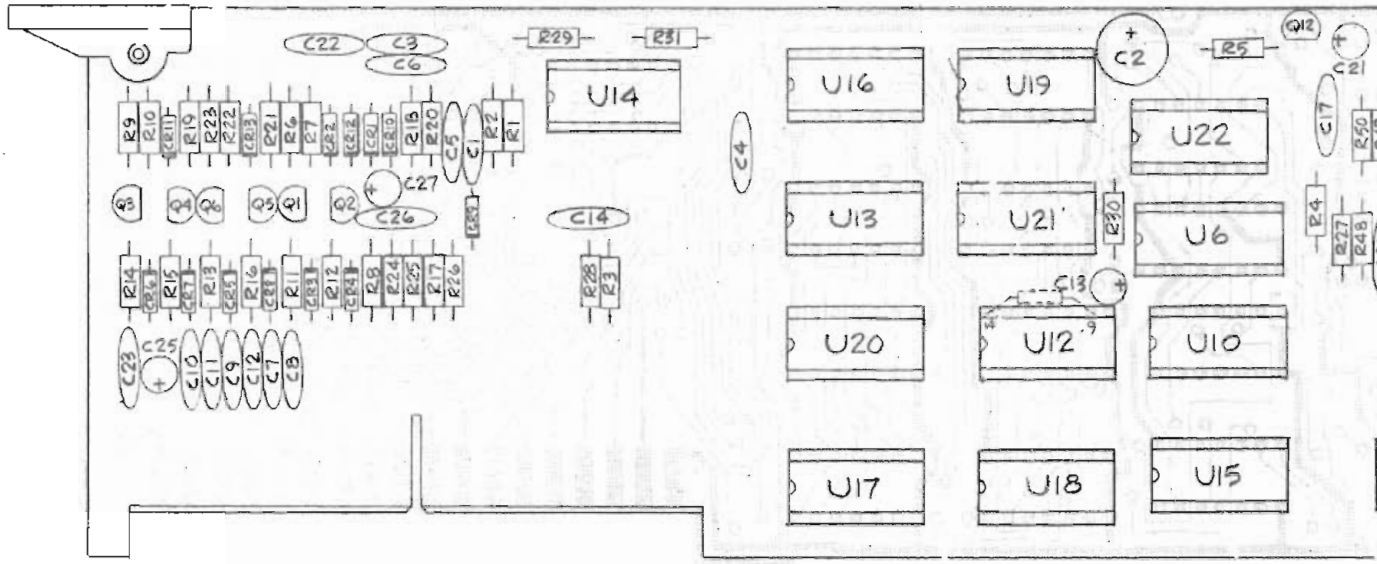


IC	TYPE	GND	+5V	-5.2V
U1, 3, 4, 5, 14	DM74LS257N	8	16	
U2	DM74LS04	7	14	
U6, 7, 8, 9, 10, 11, 12	DM74LS75	12	5	
U13	DM74H11P	7	14	
U15	94C10125L	16	9	8
U16, 17, 18	DM74176N	7	14	
U19	DM74LS490	8	16	
U20, 21	DM74196	7	14	



5500083 A
July 1979

FIGURE 9-5B
SCHEMATIC DIAGRAM
COUNT CHAIN (A103)



CONTROL (A104)

General

The primary function of this unit is to control and step the counter through the sequence of operations required to measure the frequency of the input signal to the counter.

As with the central processing unit of a computer, generation of this sequence of commands to various portions of the counter is timed by an internal clock. The sequence may be modified by external control inputs, hence the outputs of most panel controls on the counter feed directly to this unit (TEST, BAND, RESET, etc.). Reset always returns the sequence immediately to a fixed starting point.

Control Sequence Generator (U1-5)

This unit produces control signals in sequence on one of sixteen output lines. U5 is a straight scale-of-sixteen binary counter which advances one state each time a clock pulse is applied to its input. The four outputs A, B, C, and D, are applied to two 3-8 line decoders (U3,U4) to produce an output on one of 16 lines corresponding to each of the sixteen possible states of binary counter U5. A reset signal to U5 returns the unit to the start of the sequence with the "0" output line active. A disable input to the decoders allows all outputs to be deactivated at any point in the sequence. This is used during the clock pulse or the reset input to U5 to prevent false outputs on any decoder lines from occurring during times when the counter outputs are in transistion between states.

Flip-flop U2A is used to indicate whether the sequence is in one of the states "0" through "9" or in one of the states "10" through "15". After state "9", the frequency measurement is already complete but not yet displayed. The reaction to external interrupts is then different in these two cases.

Flip-flops U1A and U1B are used to produce a much longer than normal step in the control sequence. This allows extra time to read data from the DCU's of the Count Chain in A103 through a multiplexer into latches which hold this data. Output state "11"" sets flip-flop U1A which immediately gates off all the decoder outputs via gates U10B, U9B, U11A, and U11B. The sequence generator then operates at full speed in states "12" through a second "12". Flip-flop U1B is set by the D output of U5 while going into state "8", which reactivates the decoder outputs. The output during state "12" is able this time to reset both U1A and U1B, and return the sequence generator to normal operation. The DATA UPDATE output during this long step of the sequence is obtained from U1A rather than from the decoder outputs.

Decoder outputs "13" and "14" are combined in U16 to produce a Print Command pulse twice the duration of the normal sequence outputs.

The control sequence may be frozen in any state by interrupting the clock input to binary counter U5.

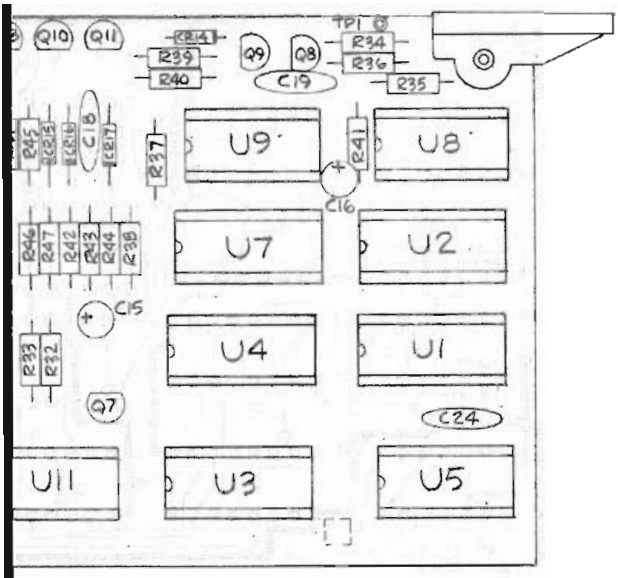
Control Sequence

There are 16 output lines from the decoders which are energized in sequence each time the counter repeats a measurement cycle. The operations which correspond to commands on each of these lines 0-15 are listed in Table 9-6A.

Any of the normal times listed the Table may be extended by interrupting the sequence clock. The times listed as variable in the Table are controlled by internally generated interrupt signals. With Programming Option P4, such an interrupt may be applied from outside the counter. This might occur with a printer, which must freeze the data in the counter until printing is complete. Other interrupts may be generated internally, depending upon the state of the input signal to the counter.

Control Sequence Reset or Interrupt Conditions

The Sequence Generator is reset to its "0" state in a variety of conditions where a measurement has started but cannot be successfully completed. The reset then prevents erroneous data from being displayed or sent out to other remote equipment. The actions that cause these resets include: externally controlled changes of the mode in which the counter operates (band change, Test, etc.), or large changes in the input signal itself before a successful measurement can be completed. The sequence can also be interrupted or reset by direct external commands.



2020074 J
9/78

Events which cause both reset of the sequence to "0" and Converter recycle (plus immediate zero display), are as follows:

a. Counter power turn-on.
b. Switch to Band B.
c. End Test in Band B.
d. Reset commands externally or manually applied.

Other events which cause the sequence to be reset to "0":

a. Change of RESOLUTION controls.
b. Switch to Band A.
c. Start Test.
d. End Test in Band A.
e. Start-cycle command from external source.
f. Converter lock or unlock in Band B during sequence "0" - "9".
g. PRF limit signal changes state (input signal appears or drops out) during sequence "0" - "9".

A number of conditions also cause the sequence to be inhibited:

a. A direct Sequence Inhibit command from an external source.
b. Operation of the Display Time Generator. This produces a variable time inhibit controlled by the SAMPLE RATE control or a permanent inhibit with the control at HOLD. A reset (external or manual) command over-rides this signal and causes a single sequence before the inhibit is re-established.
c. Operation of the Gate Generator (A105). During Sequence "8" if the counter is in Test or locked to an input signal, the Gate Generator inhibits the sequence until the prescribed gate time is accumulated. Input signal dropout removes this inhibit unless the unit is in the Test mode.
d. PFR limit signal appears (input signal level above threshold) in Band B, but Converter LOCK absent. A delay is produced before sequence continues (or resets) to see of Lock will soon be achieved.
e. LOCK lost in Band B. Time is allowed for relock to a measurable input signal before a reading of zero is produced. This prevents zero readings when lock is broken, even though a measurable input is present continuously.

Reset Pulse Trigger Generators

A large proportion of A104 consists of circuits which reset the sequence generator or other portions of the counter. The triggers which operate the reset generators are formed from the various inputs in the same way. The input signals are step functions which are differentiated in RC networks (C16, R37, for example), and coupled through diodes to a common two transistor output stage (Q10, Q11, for example). The TTL compatible output trigger then drives the IC reset generator or gate.

Six inputs to C7-C12 are combined in diodes CR3 - CR8 and output stage Q3, Q4 to reset the sequence generator through gate U11D. Four additional inputs to C3-C6 are combined in CR10-CR13 and output stage Q5, Q6 to drive OR gate U22A. During sequence states "0" - "9", this gate drives the first network through CR9 and resets the sequence generator if any input to C3-C6 occurs during states "0"-"9".

Three inputs to C17 - C19 drive a similar network through CR15 - CR17, and Q9, Q9. These trigger the reset generator one-shot U7A, which produces a uniform pulse about 5 μs in duration. This pulse resets the sequence generator, the display generator, the lock delay generator, and externally the Count Chain and Converter. The Count Chain immediately generates and displays a zero.

The inputs to C18 and C19 are obtained from Schmitt triggers in U9. Inputs to U9 are slow rise signals which are changed to single fast steps by the threshold circuits of U9.

FIGURE 9-6A
COMPONENT LOCATOR
CONTROL (A104)

SEQUENCE	FUNCTION	DURATION
0	Reset - Resets "0" - "9" Detector.	10 μs
1	Reset - Counting Chain reset to zero.	10 μs
2	Offset Load - Last three DCU's of Count Chain set to any desired number.	10 μs
3	Blank	10 μs
4	Blank	10 μs
5	Blank	10 μs
6	Reset Time Base Generator - Resets Time Base Flip-flop and accumulator on A105.	10 μs
7	Blank	10 μs
8	Signal Gate Enable - Allows Gate Generator (A105) to open the signal gate for the prescribed gate time in response to indication of a measurable input signal to the counter. This is the period when the measurement of input signal frequency actually occurs.	Variable
9	Blank	10 μs
10	Measurement complete - Sets "0" - "9" Detector to show that measurement portion of cycle is complete.	10 μs
11	Update Data - Latches associated with each DCU of the counting chain are latched to new DCU data.	170 μs
12	End Update Data - Resets update data flip-flops.	10 μs
13 14	Print - Sends out signal indicating that new measurement data is available.	20 μs
15	Display - Starts variable time delay, controlled by SAMPLE RATE control, which separates successive measurement cycles.	Variable

TABLE 9-6A. CONTROL SEQUENCE

Display Time Generator

After each measurement is complete, this unit inhibits the Sequence Generator for a time interval determined by the front panel SAMPLE RATE control. In the HOLD position, the inhibit is permanent until a manual or external reset command is applied, or the power is turned off.

The generator includes a variable period one-shot U7B and DCU U8. The one-shot is connected to produce a free running multivibrator during the delay time. Its output drives the DCU, which extends the period of the one-shot by a factor of ten. The only output of the display generator is a sequence inhibit signal. The DCU outputs are combined to inhibit the sequence, in all but the DCU "9" state. This signal is further combined with the sequence "15" and Fast Cycle controls so that inhibit can occur only in sequence "15" with Fast Cycle not applied and with the display generator DCU not in the "9" state. The Hold input keeps the DCU at "0" state, which applies a permanent sequence inhibit in sequence state "15" as long as Fast Cycle is not applied (or the unit reset).

To start the display time, the DCU is set from the previous "9" state to "0" during Sequence "14". At Sequence "15", the display time one-shot is triggered and commences to free run at a rate determined by the SAMPLE RATE control setting (approximately .3 - 30 pulses per second). Unless held reset by a Hold command, the DCU is stepped at this same rate until it reaches state "9". The sequence inhibit is then removed and the sequence continues normally, thus ending the display time.

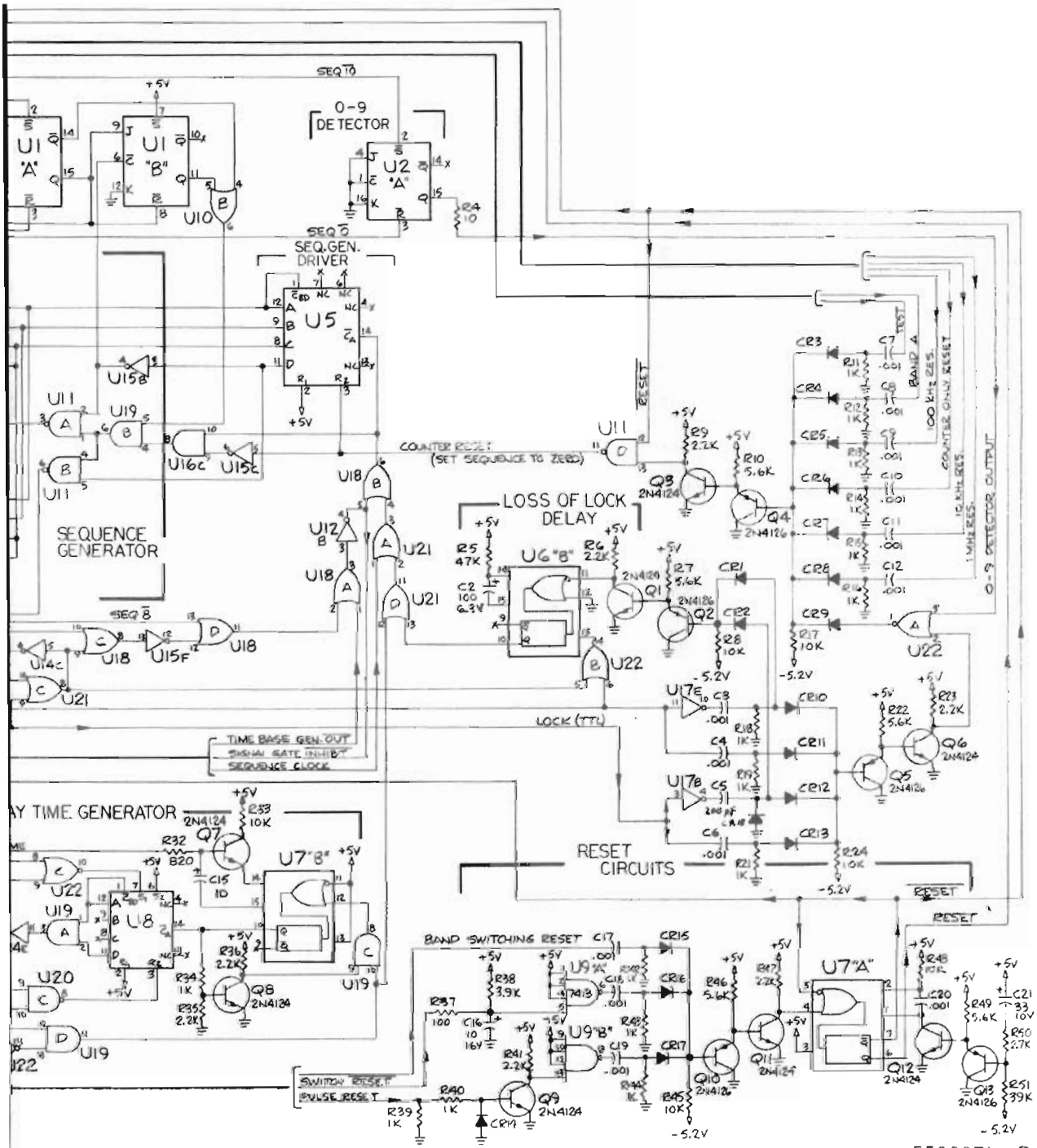
Test Mode

The circuits involved in test mode generation are primarily Test Flip-flop U2B. The input command is inverted and drives the flip-flop into the set state. It is held in this state until the input command is removed. Sequence Generator "15" output then resets the flip-flop at the end of the measurement cycle. Outputs of the flip-flop reset the sequence generator at start and finish of TEST, supply TEST commands to the Gate Generator (A105) and the High Frequency (A106) boards, remove the Offset Load command in Band B, and remove the Band A and B control signals to A106. The outputs provided cause the counter to measure an internal 200 MHz test signal as long as the Test Flip-Flop is held set.

PRF Limit

The PRF Limit circuits receive the input threshold signal from Gate Generator A105. This signal is present whenever the input signal to the counter is above the preset threshold level, and absent when it is below this level. The PRF circuit then produces a continuous output unless gaps in the input exceed about 100 ms, indicating a dropout of the input signal. The PRF Limit Disable input, when active, causes the PRF circuit to produce a permanent high output, despite the disappearance of the input signal.

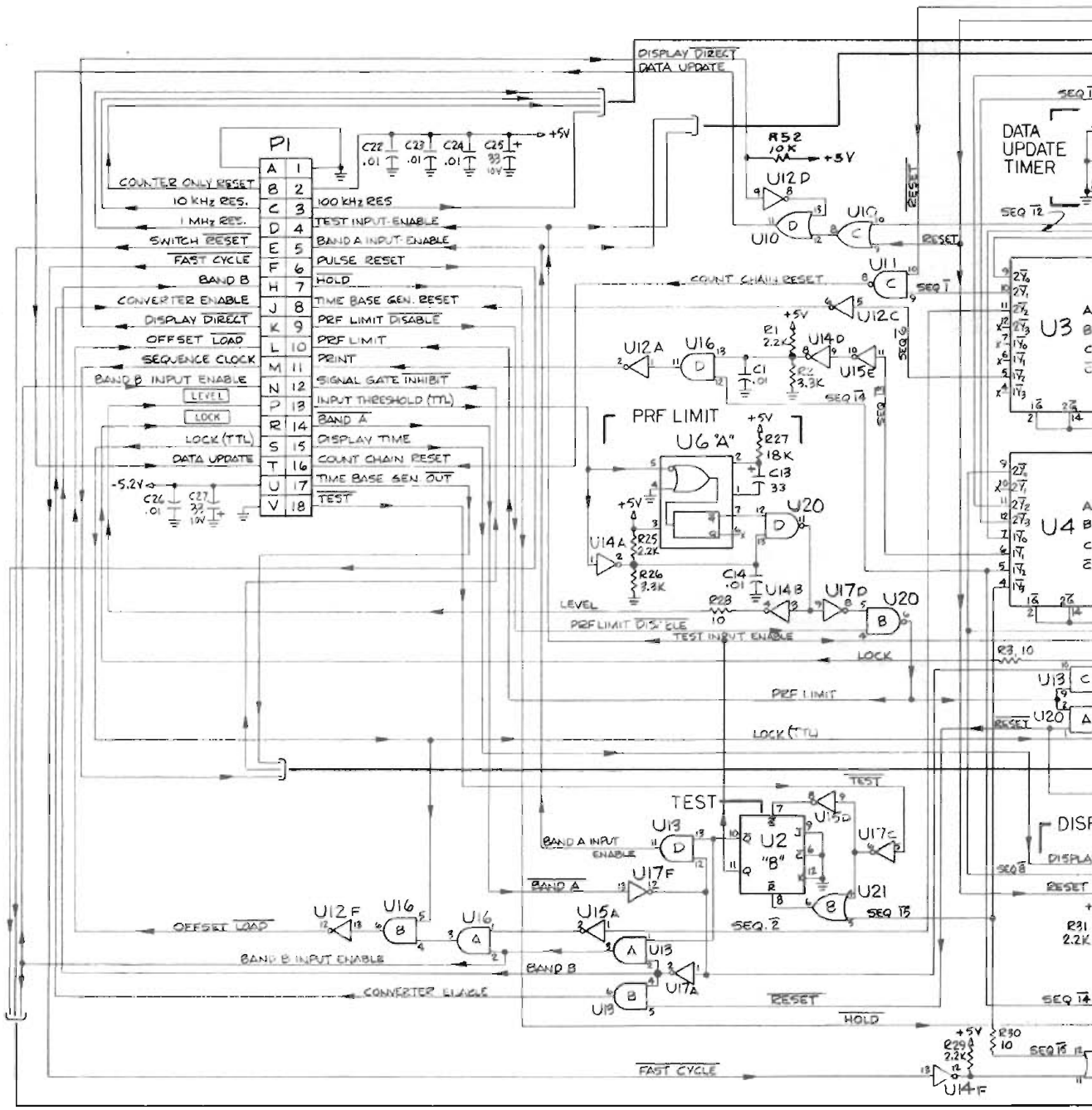
The PRF circuit includes a one-shot (U6A), triggered by the step which occurs when the input threshold signal disappears. The threshold signal also produces a fast-fall, slow-rising output from inverter U4A with C14, R25, and R26 load. This signal and the one-shot Q output are combined in NAND gate U20D to produce a signal that rises rapidly with appearance of the threshold signal. It does not fall however, unless the threshold signal stays low for more than 100 ms (the time constant of the one-shot.)



5500074 D

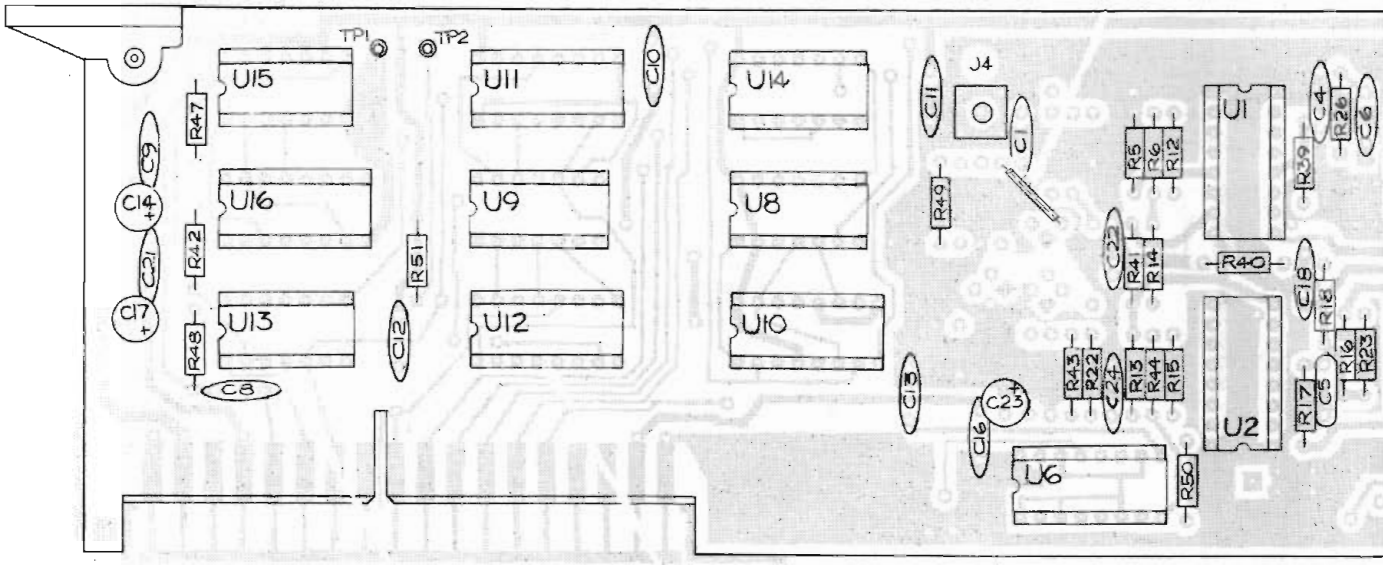
July 1979

FIGURE 9-6B
SCHEMATIC DIAGRAM
CONTROL (A104)



IC	TYPE	GND	+5V
U1, 2	DM74LS76	13	5
U3, 4	DM74LS155	8	16
U5	DM74LS93	10	5
U6, 7	DM9602N	8	16
U8	DM74LS90	10	5
U9	DM74LS13	7	14
U10, 18, 21	DM74LS32	7	14
U11, 20	DM74LS00	7	14
U12, 15, 17	DM74LS04	7	14
U13, 16, 19	DM74LS08	7	14
U14	DM74LS05	7	14
U22	DM74LS02	7	14

BOX ☐ DENOTES FRONT PANEL INDICATOR.
ALL DIODES ARE IN4154.



GATE GENERATOR (A105)

General

The primary function of this unit is to produce the gate signal which controls the time intervals over which the input to the counter is accumulated. It also produces the 100 kHz Control Sequence Clock, and a 200 MHz Test signal. These outputs are all based on 200 MHz and 10 MHz references supplied from other portions of the counter.

Gate and Enable Flip-Flops (U2A/B).

The flip-flops are dual ECL types, both clocked by the same 200 MHz reference signal. The Gate Flip-flop controls the main counter signal gate directly, while the Enable Flip-flop determines which cycle of the 200 MHz clock will trigger the Gate Flip-flop.

The enable signal to the Enable Flip-flop, is derived from the counter input threshold circuit, and is present only at times when an input signal of adequate amplitude is present. This signal is combined with a signal from Control board A104, which indicates that the counter is in the correct part of its cycle to actually measure the input signal frequency. The rise time of the enable signal is faster than the clock period, so the Enable Flip-flop will always settle definitely into one of its two stable states when any individual clock pulse arrives.

The output of the Enable Flip-flop is applied to the enable input of the Gate Flip-flop which is triggered to the corresponding state by the next 200 MHz clock pulse. Transistions of the Gate Flip-flop occur only at a defined trigger point on the clock pulse, which is timed very accurately (< < 1 ns from periodic 200 MHz). The output of the Enable Flip-flop is also combined with the output of the Time Base Flip-flop (U2B). This allows only a specified number of clock pulses to occur during the gate time of each measurement cycle of the counter. Accumulated gate times are: 1 ms or 100 µs (4 ms or 400 µs in Band A). The Gate control signal is applied via a 50 ohm cable to the signal gate on A106.

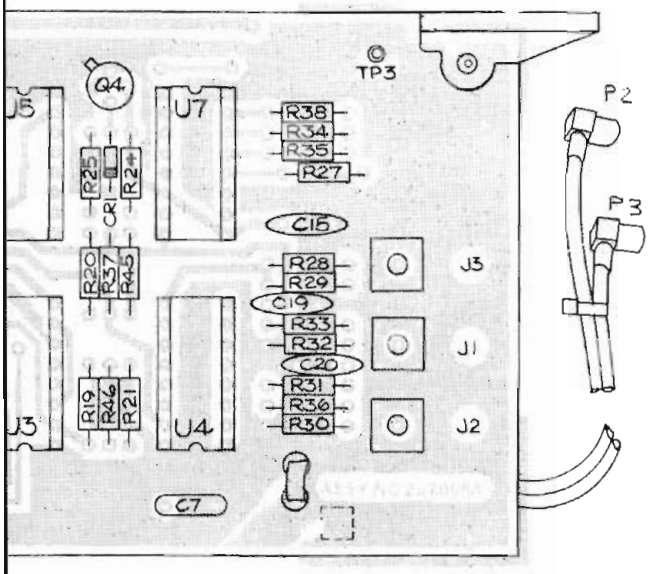
Time Base Flip-Flop (U3B).

This is another fast ECL flip-flop. It is clocked by a 200 MHz signal, slightly delayed from that driving the Enable and Gate Flip-flops. The delay allows the Gate Flip-flop (triggered by the normal clock), to control the delayed clock during the same clock period in which the Gate Flip-flop changes state. The clock delay and propagation delay through the flip-flop, are approximately equal. The Time Base Flip-flop is reset at the beginning of each measurement cycle, removing the disable signal applied by it, to the Gate Flip-flop.

During the gate enable portion of the counter control sequence, the Gate Flip-flop is controlled by the input threshold circuits via the Enable Flip-flop and the 200 MHz clock. Each time the Gate Flip-flop opens the Signal Gate, the 200 MHz delayed clock is also applied to the Time Base Accumulator and to the Time Base Flip-flop clock input. The clock pulse which opens the signal gate is ignored. All pulses which occur during a Signal Gate open period are recognized, including the one which closes the Gate. Coincidence circuits in the Time Base Accumulator produce signals when N-4 and N-3 clock pulses have been applied to the Accumulator. N is the number of clock periods required to produce the desired accumulated gate time. The N-4 signal is applied to the clock enable input, and the N-3 signal to the enable input of the Time Base Flip-flop. The N-2 clock pulse then actually triggers the Time Base Flip-flop to its set state. The delay already present in the delayed clock driving the accumulator, is extended by a delay network following the Time Base Flip-flop. The disable signal from the Time Base Flip-flop to the Gate Flip-flop input is then delayed until after the N-1 normal clock pulse. The N clock pulse resets the Gate Flip-flop, and ends gate time for that measurement cycle.

Time Base Accumulator (U3A, U5, U10-12)

The Time Base Accumulator includes five DCU's (U5, U11, U12), preceded by a binary divider. The count capacity of this group is 200K clock pulses, each of 5 ns period, or



2020085 F
9/78

1 ms total. The last DCU may be removed from the string to permit a 100 µs gate time. In addition to the string of DCU's, a ÷4 unit is included between the first and second DCU's, which may be switched into or out of the chain. The ÷4 is included when operating in Band A, to increase the gate time by a factor of four. The input to A106 is divided by four before reaching the Signal Gate, so the gate time must be extended to cause the counter to read the input frequency directly.

A coincidence detector consisting of U7A, U8, U9, U14D, Q4, CR1, and the D output of U5, produces an output when all DCU's of the string are in state "9", and the ÷4 unit is in state "3". The first DCU of the string is preset to 9 originally, giving coincidence after N-2, rather than N-1 clock pulses to the first DCU. (Driving C_{BD} input with the A, rather than the inverted A output, is equivalent to a preset 9.) Since the accumulator clock input is divided by two in binary U10A before the first DCU, coincidence output occurs on the N-4 input pulse.

Since coincidence occurs when all DCU's are at 9, and the ÷4 at 3, any one of them is effectively removed from the string if held at these counts. U12B has an external set 9 input to produce the shorter 100 µs gate time in this manner. This ÷4 unit may also be held at 3 by an external control signal (Band B or Test), but additional gating must be provided to pass the input signal around the stage, since the following DCU's still have to operate. This is accomplished in U8B, which transmits either the input or output of U10 to the input of U11A.

The ÷2, and the first DCU of the Accumulator, are fast ECL circuits, able to divide the 200 MHz clock to 10 MHz; the remaining circuits are TTL.

Band Select Circuits (U4B-D, U7B/C, U14A)

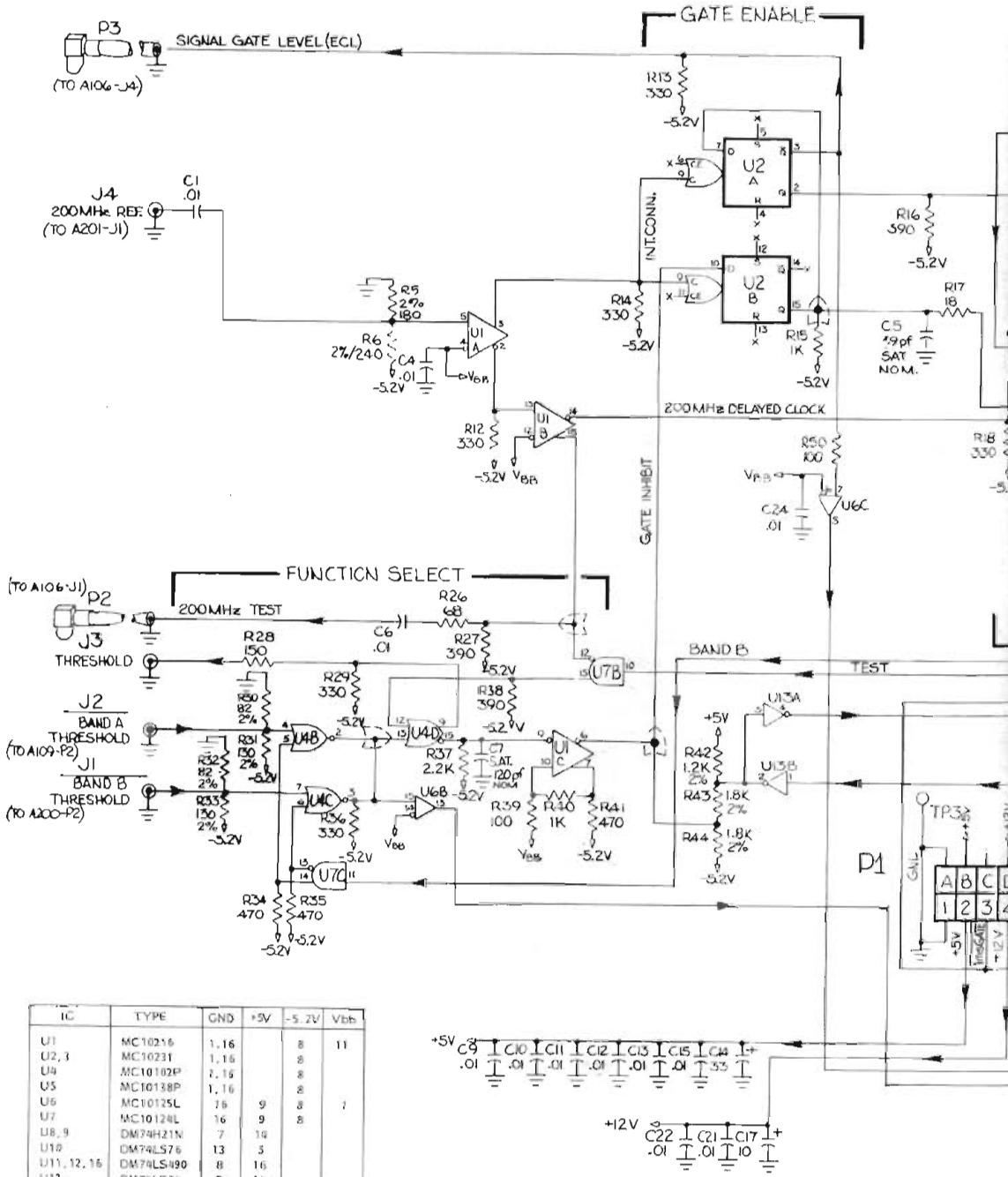
These circuits select one of the Band Threshold signals from either the Converter (Band B) or Prescaler (Band A), and processes this to control the Enable and Gate Flip-flops. U7C is simply a buffer/inverter which is driven by a level derived from the front panel BAND SELECT switch. The buffer output drives one input of U4B, while the inverter output drives one input of U4C, such that one of the pair U4B/U4C is always enabled, and one disabled. The inverting outputs of U4B and U4C are "ORed" together to drive one U4D input. The direct out- of U4B is now a replica of the envelope of the signal to the selected input to the counter — being high if the signal is above threshold level, and low if the signal is less than threshold. The second input to U4D is high in the Test mode, so the Gate Flip-flop operates as if the 200 MHz Test signal is always above threshold level.

The output of U4D to the Enable Flip-flop goes low whenever the input signal to the counter is above threshold. A capacitor to ground slows the fall of this transistion without great effect on the risetime. The signal is squared up again in U1C to produce an Enable signal which is delayed from the rise of the input signal to threshold, but disappears without delay as the input drops below threshold. This delays counting of the input signal until irregularities on the rise of the RF pulse have died out.

Control Sequence Clock Generator (U14-16)

This circuit divides the input 10 MHz reference by 100 to form the 100 kHz Sequence Clock. The input accepts a wide variety of input levels and waveshapes, while producing a square wave of the proper level to drive U16. U15B gates the outputs of U16 to form 100 ns pulses at a 100 kHz rate. U14C allows the Clock to be gated by an external control level.

FIGURE 9-7A
COMPONENT LOCATOR
GATE GENERATOR (A105)



IC	TYPE	GND	+5V	-5.2V	Vbb
U1	MC10216	1, 16		8	11
U2, 3	MC10231	1, 16		8	
U4	MC10102P	1, 16		8	
U5	MC10138P	1, 16		8	
U6	MC10125L	16	9	8	7
U7	MC10124L	16	9	8	
U8, 9	DM74H21N	7	14		
U10	DM74LS76	13	5		
U11, 12, 16	DM74LS490	8	16		
U13	DM74LS04	7	14		
U14	DM74LS02	7	14		
U15	DM74LS13	7	1		

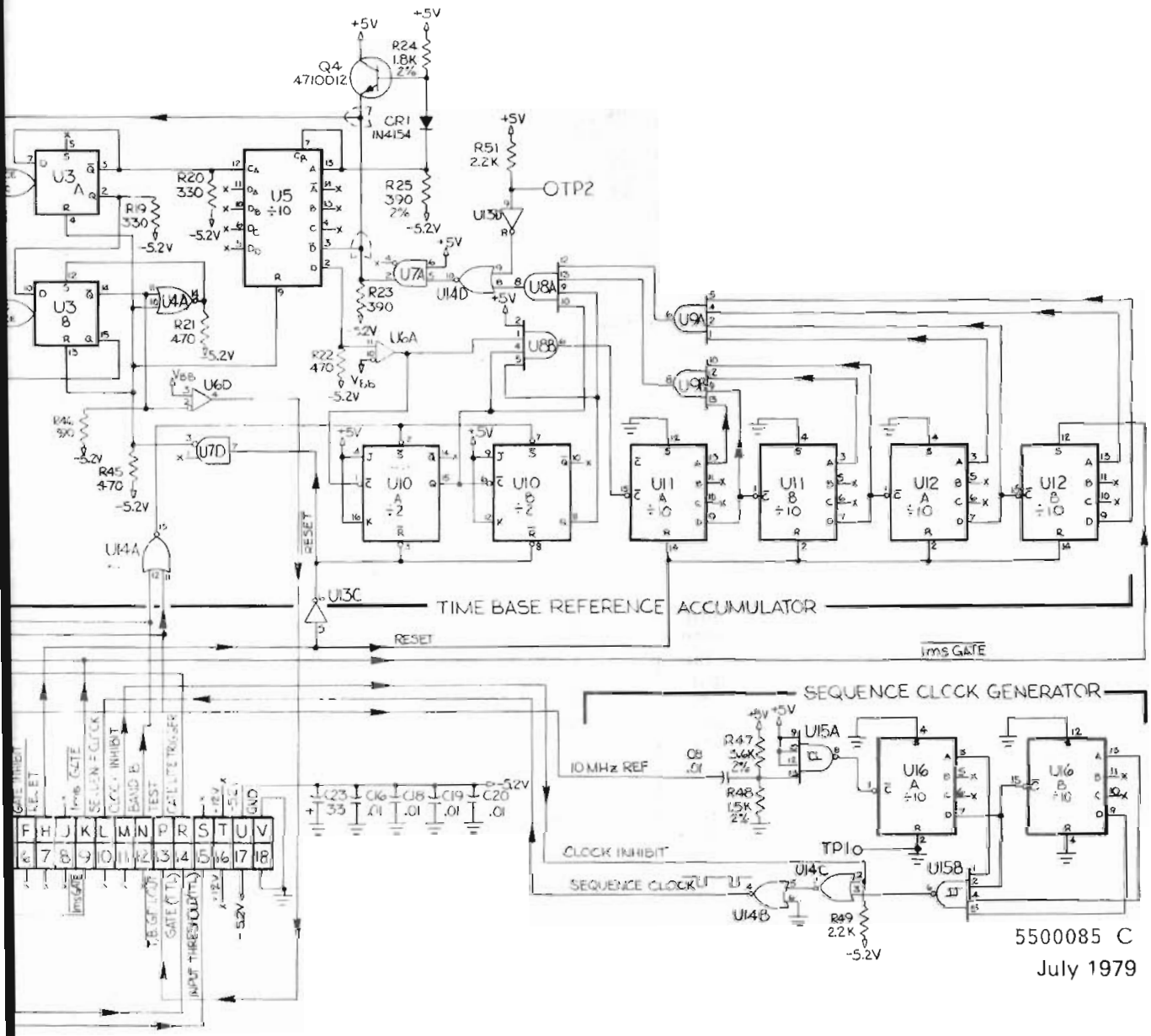
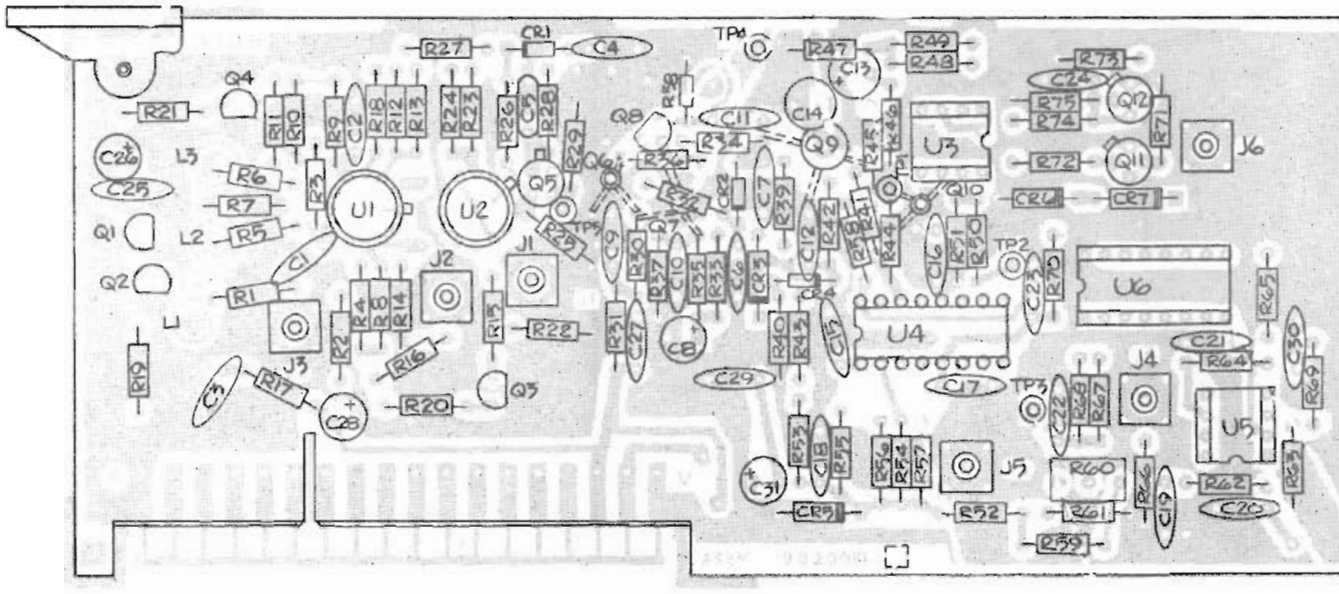


FIGURE 9-7B
SCHEMATIC DIAGRAM
GATE GENERATOR (A105)



HIGH FREQUENCY (A106)

The High Frequency board provides the initial signal processing and first decade of counting for the Direct Counter. It selects and processes one of three input signals: the Converter IF output, the Prescaler divide-by-four output, and the 200 MHz Test signal. BCD information and the divide-by-ten output from the first decade counting unit are sent from this board to the Count Chain board (A103) for further counting and display.

One of the three input signals is selected by enabling one of three differential amplifiers: U1B, U2A, or U2B. U1A provides additional gain for the Converter IF signal when input U1B is selected. Enabling of the appropriate amplifier is achieved by activating transistor Q2, Q3 or Q4, by TTL Band Select commands entering on P1.

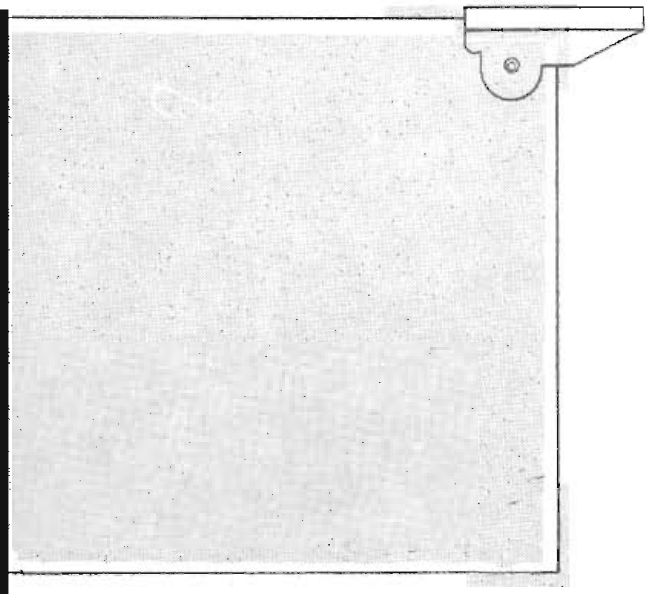
The output of the input selector differentially drives the squaring circuit. Q5 is a current mirror, which is used as as an overdriven voltage-to-current converter. The collector current of Q5 drives the pulse forming network which begins with a wide-band, high-speed differential amplifier (Q6/Q7). The output of this differential amplifier drives Q8, which is used as a current switch. The resulting current square wave from Q8 drives inductor L4, producing a series of pulses — a positive pulse when Q8 turns on, and a negative pulse when Q8 turns off.

The pulse inverter is essentially a high-speed zero bias amplifier. Q9 performs this function by being biased at cut-off by diode CR4. In this mode, the amplifier not only inverts the positive pulses, but removes the unwanted negative pulses. The output of the pulse inverter drives the input of decade divider U4. The bias point for U4's input is established by a tracking bias supply (U3/Q10). The output of U3 is equal to the voltage on U4 pin 1, plus a fixed DC offset selected by resistor divider R47/R49. The divide-by-ten output of the decade divider is a 60/40 duty cycle ECL level signal called "DCU CARRY". The load resistor for this signal is located on the Count Chain board (A103) to provide a termination for the connecting co-ax cable.

The BCD output information is available on P1 pins 11-14. During a count cycle at high frequencies, this information is slew rate limited, therefore the actual output levels cannot be seen until the circuit comes to rest. After the circuit is finished counting, TTL level signals are present on these outputs. The decade divider is reset after the counting cycle is complete by a TTL reset signal on U4 pin 3. This signal comes into the board via P1 pin 10.

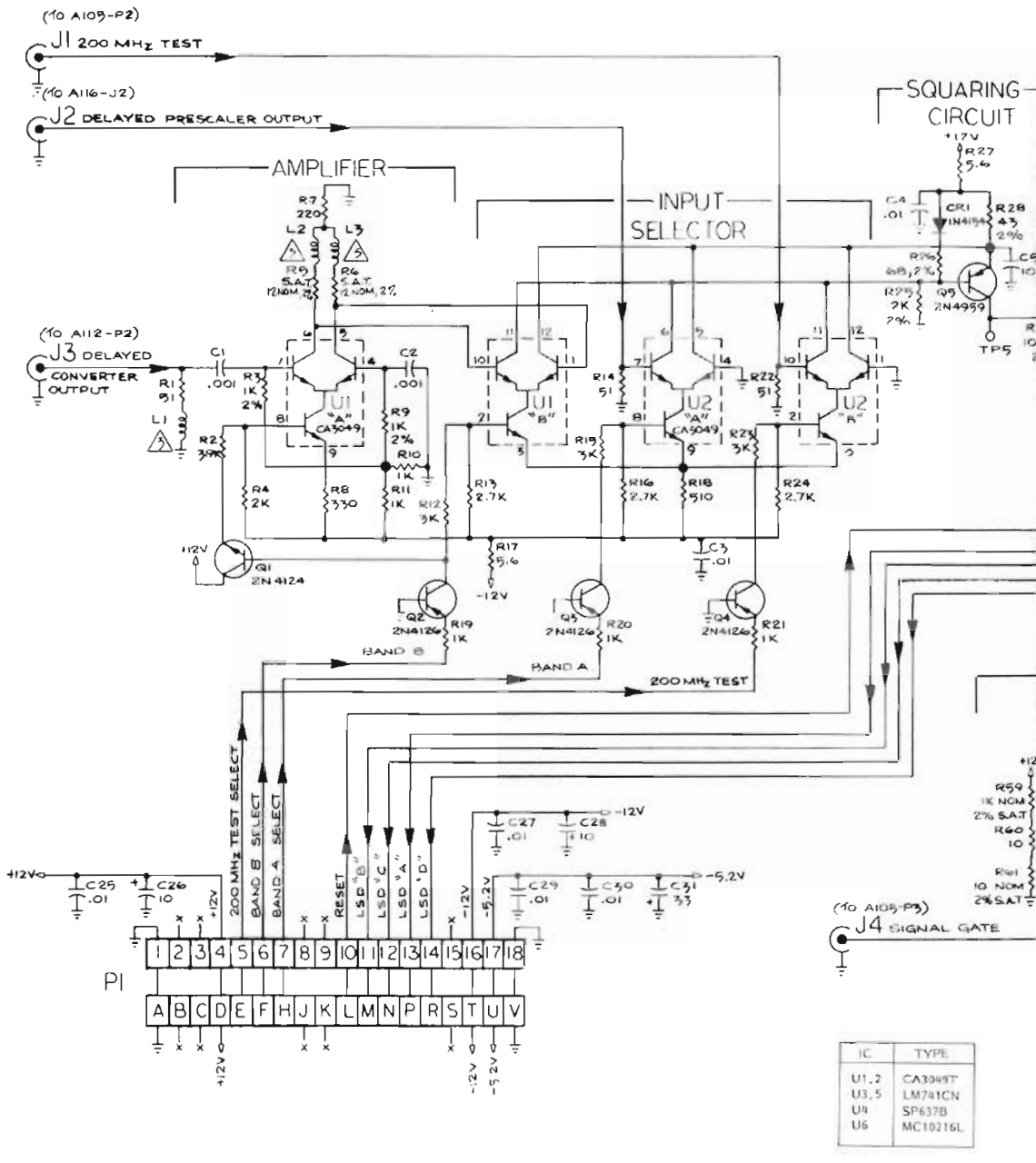
The gate signal (an inverted ECL level logic signal) enters the board at J4, and passes through U6. The first stage is an input buffer whose threshold signal (U6 pin 5) is derived from op amp temperature-compensated bias supply U5. U5's function is similar to U3 with the output tracking the reference voltage (U6 pin 11), plus some fixed offset supplied by voltage divider R59-R61. This accomodates slight changes in threshold which produce the effect of a change in gate width.

The gate output to the rear panel is supplied by the Gate Output Buffer, consisting of Q11, Q12, and associated circuitry.

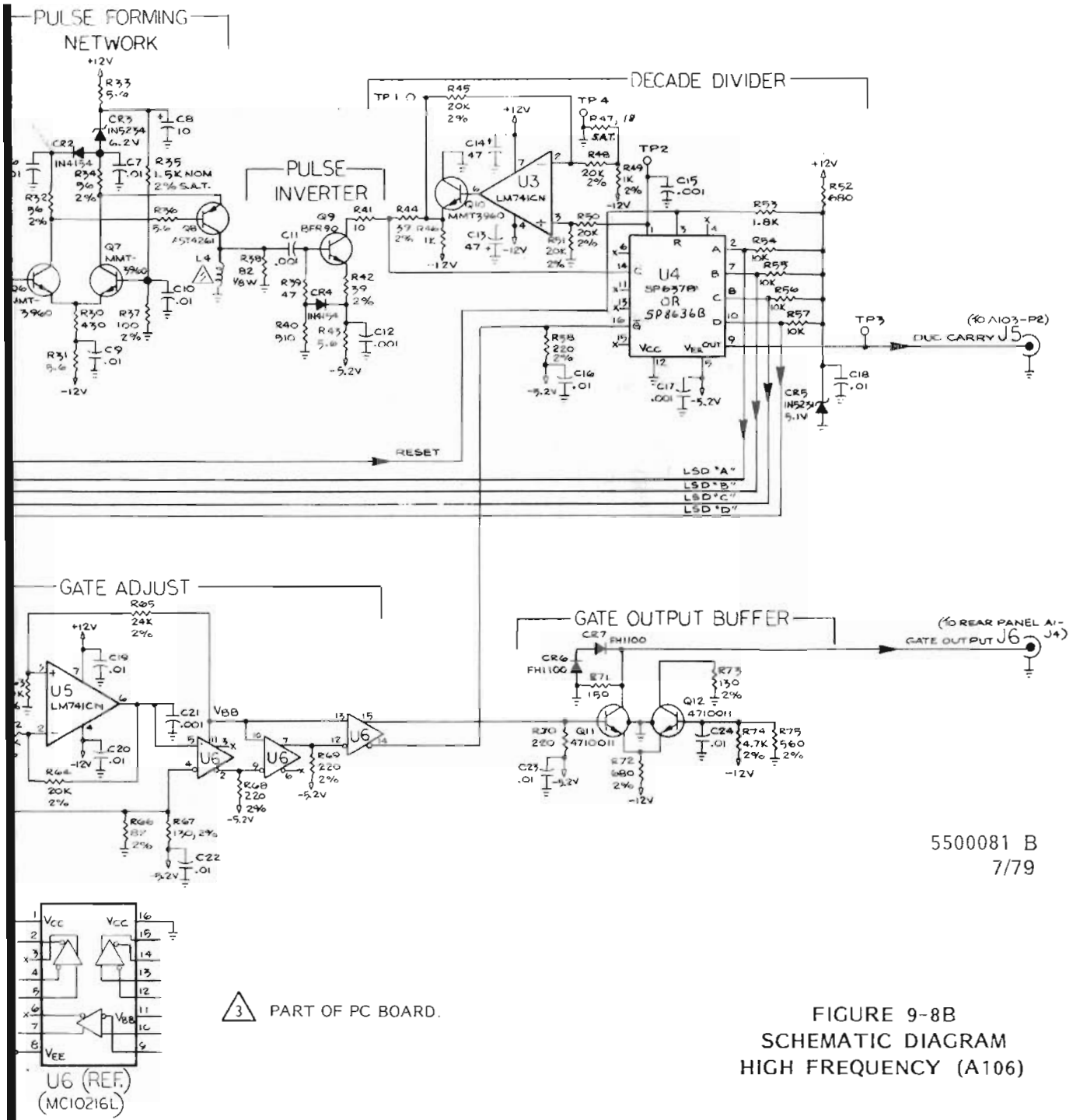


2020081 G
9/78

FIGURE 9-8A
COMPONENT LOCATOR
HIGH FREQUENCY (A106)



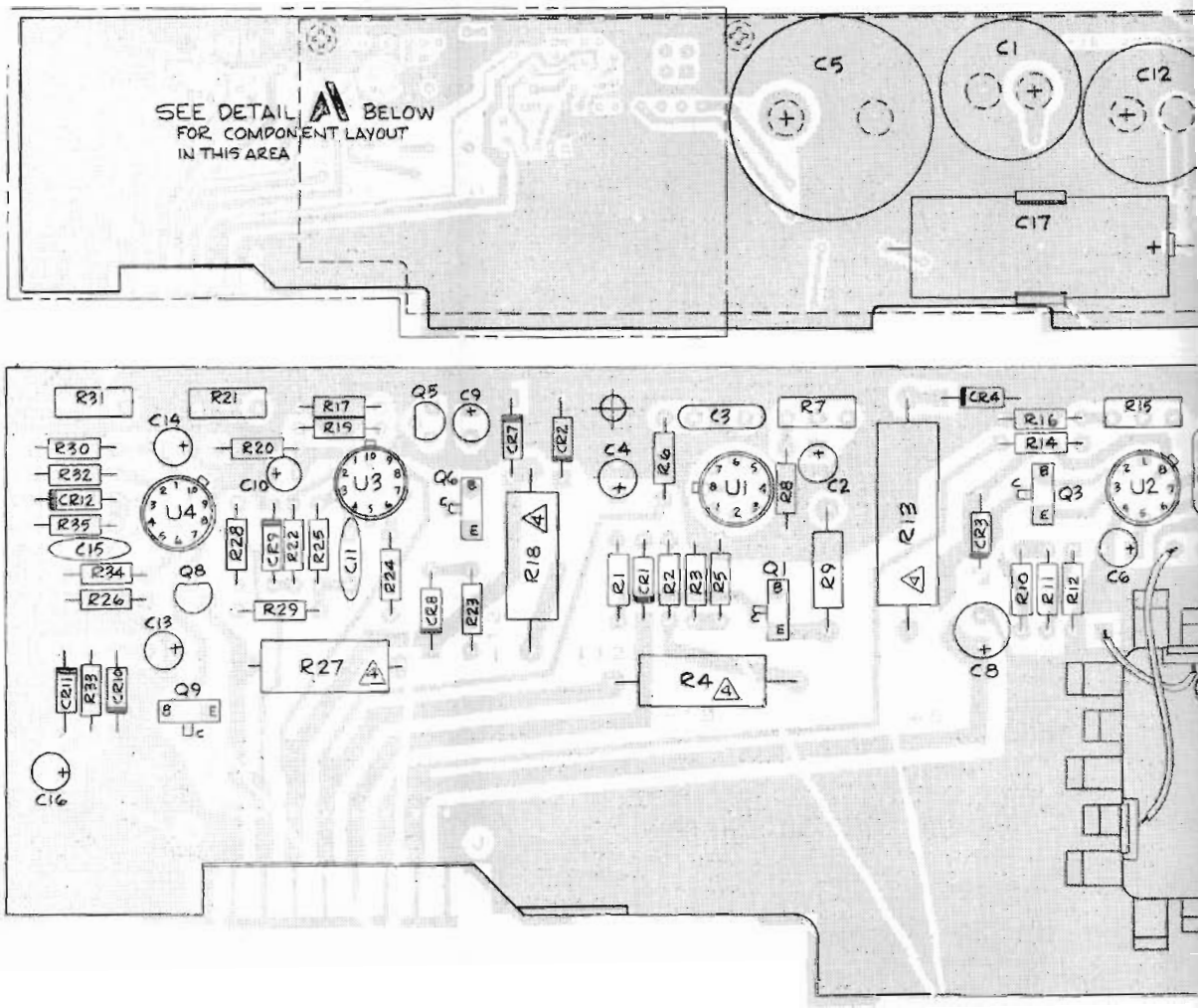
IC	TYPE
U1,2	CA3049T
U3,5	LM741CN
U4	SP637B
U6	MC10216L



5500081 B
7/79

3 PART OF PC BOARD.

FIGURE 9-8B
SCHEMATIC DIAGRAM
HIGH FREQUENCY (A106)


SEE DETAIL A BELOW
FOR COMPONENT LAYOUT
IN THIS AREA
C5
C1
C12
C17
R31
R21
R17
R19
Q5
C9
C14
R30
R32
CR12
R35
C15
R34
R26
C13
C16
R20
C10
U3
U4
R28
CR9
R22
R25
C11
R24
Q8
R29
CR8
R23
Q6
CR7
CR22
R18
C4
R6
C3
R7
U1
R8
C2
R1
CR1
R2
R3
R5
Q1
R9
R27
R4
R13
CR4
R16
R14
R15
Q3
U2
CR3
R10
R11
R12
C6
C8
Q9
CR11
R33
CR10

DETAIL A

POWER SUPPLY (A1/A107)

The Power Supply furnishes all basic operating voltages required by the counter. The supply consists of two assembly groups:

(1) PC board A107 containing the rectifiers, filter capacitors, and regulator circuitry.

(2) Chassis mounted components (A1-) consisting of the power transformer (A1T1), primary wiring, POWER INPUT module (containing the fuse, voltage changing PCB, and power input connector), and the front panel POWER switch.

Circuit Description

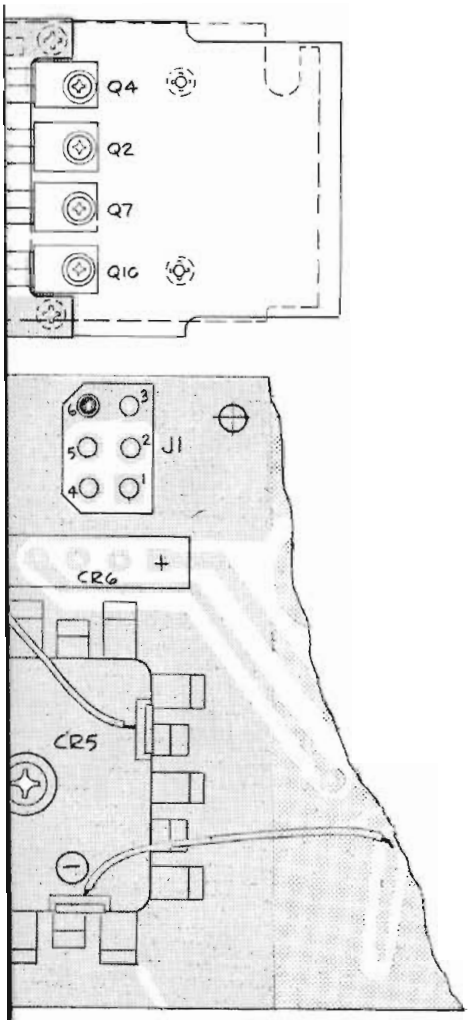
The basic voltages required by the counter are: unregulated +18 Vdc, regulated +12 Vdc, -12 Vdc, +5 Vdc, and -5.2 Vdc.

All the regulated voltages are produced by full wave rectifier and series regulator circuits. The +18 V unregulated voltage is also the input voltage for the +12 V regulator.

Each of the four regulator circuits contains an integrated circuit voltage regulator with current foldback capability, protective diodes, and provision for adjustment of the required output voltage.

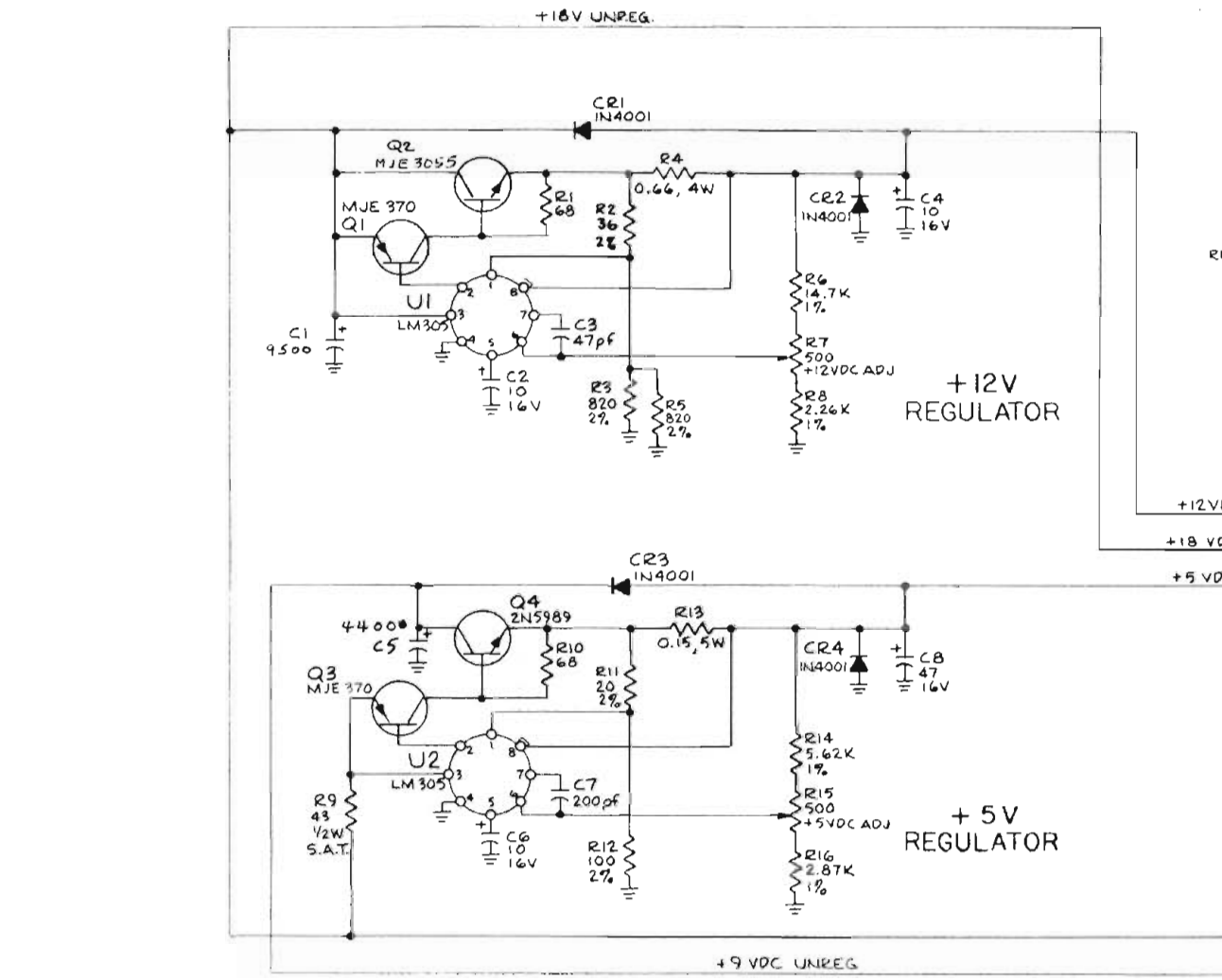
The type of IC used in both the +12 V and +5 V regulators is an LM 305. This IC contains an internal temperature compensated voltage reference, as well as the necessary circuits to provide gain and current foldback limiting. The foldback current limit control resistors in the +5 V supply (for example), are R11, R12, and R13.

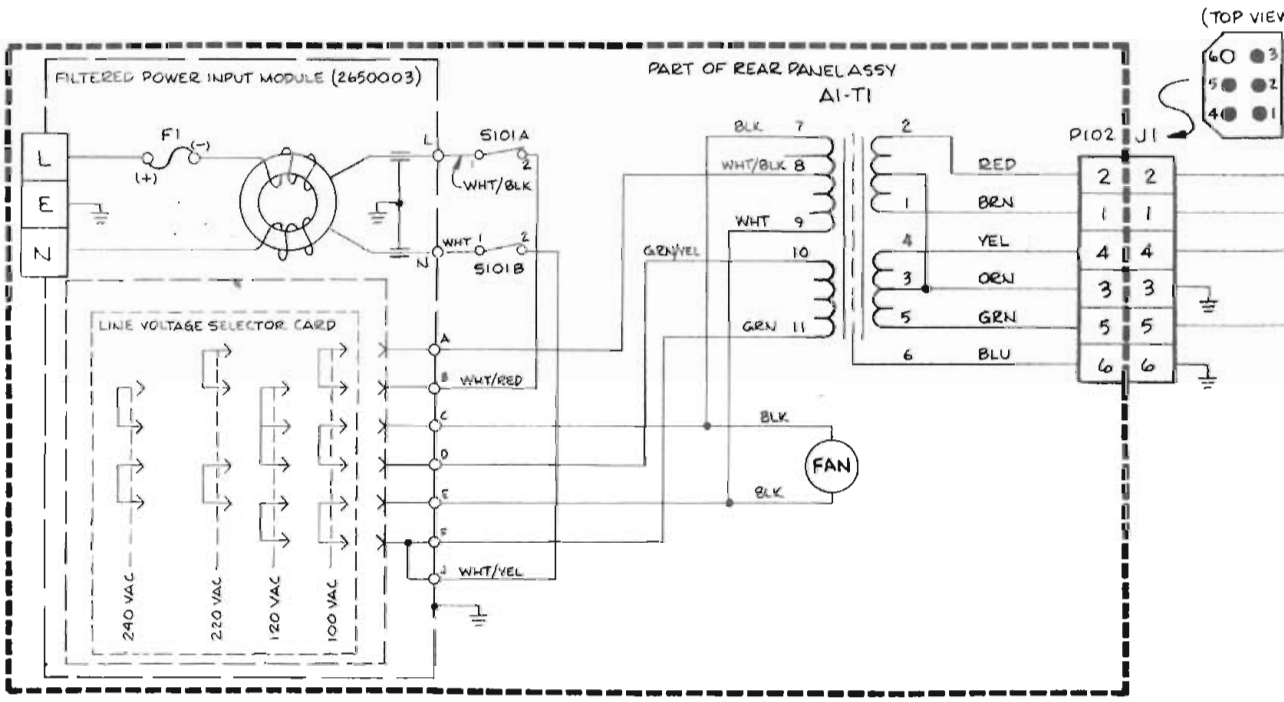
The negative supplies utilize an LM 304 as the basic IC regulator. This IC also contains an internal temperature compensated reference. To implement this reference an external pre-regulator is required. In the -12 V circuit (for example), the pre-regulator includes R22, R25, and CR9. Current foldback limiting uses internal IC circuitry in addition to R17, R18, R19 and Q5.

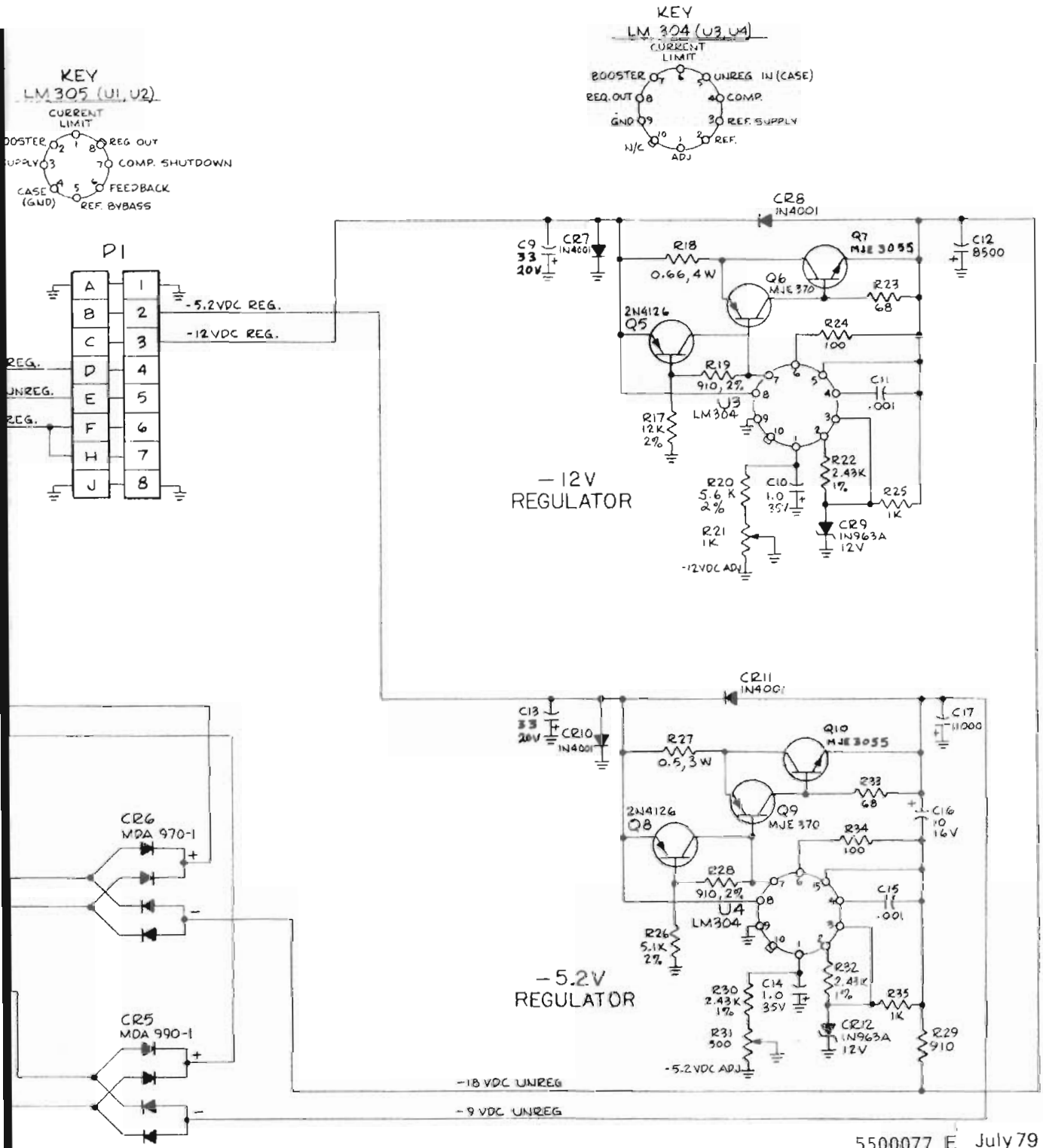


2020077 L
9/78

FIGURE 9-9A
COMPONENT LOCATOR
POWER SUPPLY (A107)

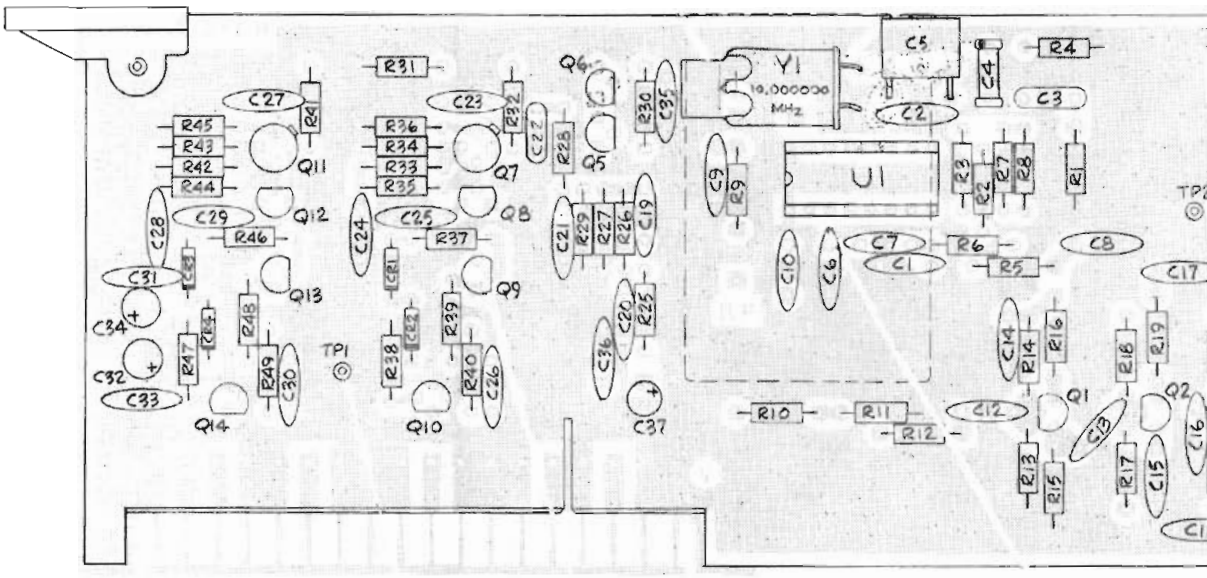

+18V UNREG.
CR1 IN4001
Q2 MJE 3055
MJE 370 Q1
R1 68
R2 36 2%
R4 0.66, 4W
CR2 IN4001
C4 10 16V
R6 14.7K 1%
R7 500 +12VDC ADJ
R8 2.26K 1%
U1 LM305
C1 9500
C3 47pf
C2 10 16V
R3 820 2%
R5 820 2%
+12V REGULATOR
CR3 IN4001
Q4 2N5989
4400 C5
R10 68
R13 0.15, 5W
CR4 IN4001
C8 47 16V
Q3 MJE 370
R11 20 2%
R14 5.62K 1%
U2 LM 305
C7 200pf
R15 500 +5VDC ADJ
R9 43 1/2W S.A.T.
C6 10 16V
R12 100 2%
R16 2.87K 1%
+5 REGULATOR
+9 VDC UNREG


(TOP VIEW)
FILTERED POWER INPUT MODULE (2650003)
PART OF REAR PANEL ASSY
A1-T1
L
E
N
F1
(+)
(-)
S101A
S101B
WHT/BLK
WHT
LINE VOLTAGE SELECTOR CARD
240 VAC
220 VAC
120 VAC
100 VAC
WHT/RED
WHT/YEL
GRN/YEL
BLK
WHT/BLK
GRN
FAN
P102
J1
RED
BRN
YEL
ORN
GRN
BLU



5500077 E July 79

FIGURE 9-9B
SCHEMATIC DIAGRAM
POWER SUPPLY (A107)


Y1
10.000000
MHz
U1
C5
C4
C2
C3
R4
R31
C27
R4
R45
R43
R42
R44
Q11
C23
R32
R36
R34
R33
R35
Q7
C27
R28
Q6
Q5
R30
C35
C9
R9
C28
C29
R46
Q12
C24
C25
R37
Q8
C21
R29
R27
R26
C19
C10
C6
C7
C1
R6
R5
C8
C17
C31
CR3
C34
Q13
CR1
Q9
R48
R47
CR4
C32
C33
R49
C30
TP1
R38
CR2
R39
R40
C26
C36
C20
R25
C37
Q14
Q10
R10
R11
R12
C12
Q1
Q2
C14
R14
R16
R18
R19
C13
R13
R15
R17
C15
C16
C11
R3
R2
R7
R8
R1
TP2

REFERENCE OSCILLATOR BUFFER (A108)

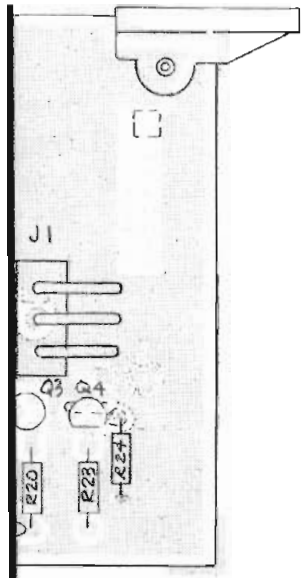
GENERAL

A room temperature, crystal controlled oscillator (RTO) is used as the basic reference against which all input signals are compared. An additional temperature-compensated crystal oscillator (TCXO) is available as Option P1, which allows the user to select a higher level of precision compatible with measurement requirements.

Circuit Description

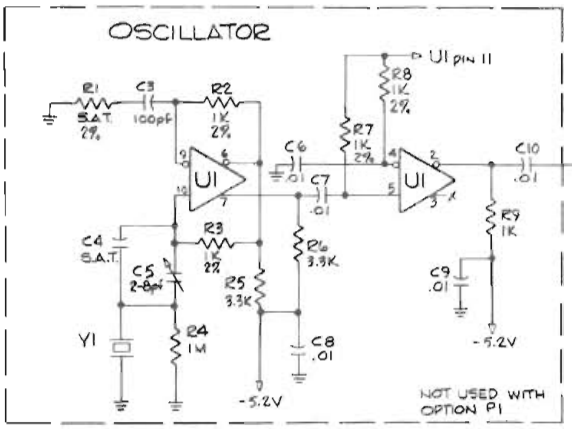
The signal from the oscillator is either a square wave from the RTO, or a sine wave from the optional TCXO. This waveform is converted to a positive-going square wave at J1 by a linear amplifier (Q1), current switch (Q2,Q3), and an output current driver (Q4).

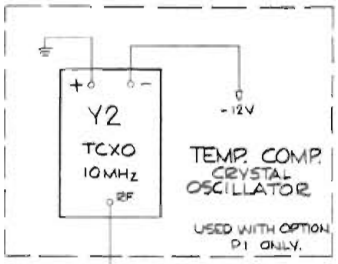
The outputs appearing at P1 pins 6 and 14, are processed by a linear, low gain amplifier pair (Q5 and Q6), and two identical line driver circuits Q7-Q10, and Q11-Q14). Low gain, common emitter input stages (Q7,Q11), are followed by emitter followers (Q8, Q12), which drive push-pull emitter follower output pairs (Q9,Q10, and Q13,Q14).

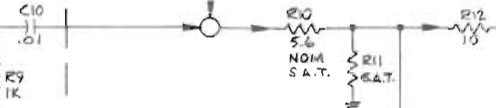


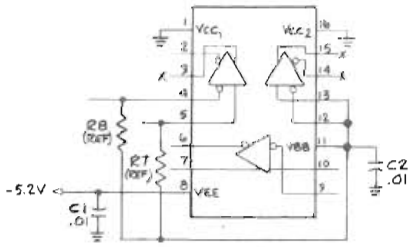
2020078 L
9/78

FIGURE 9-10A
COMPONENT LOCATOR
REFERENCE OSCILLATOR BUFFER (A108)

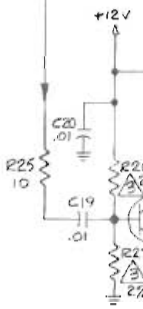








U1 (REF)
(MC10116)



REF DESIG.	STD (RM. TEMP. OSC.)	OPT P1 (TCXO)
R26	11K	9.1K
R27	1.3K	2.2K
R29	100	360
C22	33pf. S.A.T.	NOT USED

3 COMPONENT VALUES CHANGE WHEN TCXO OPTION P1 IS USED. SEE TABLE FOR CORRECT COMPONENT VALUE FOR EACH APPLICATION.

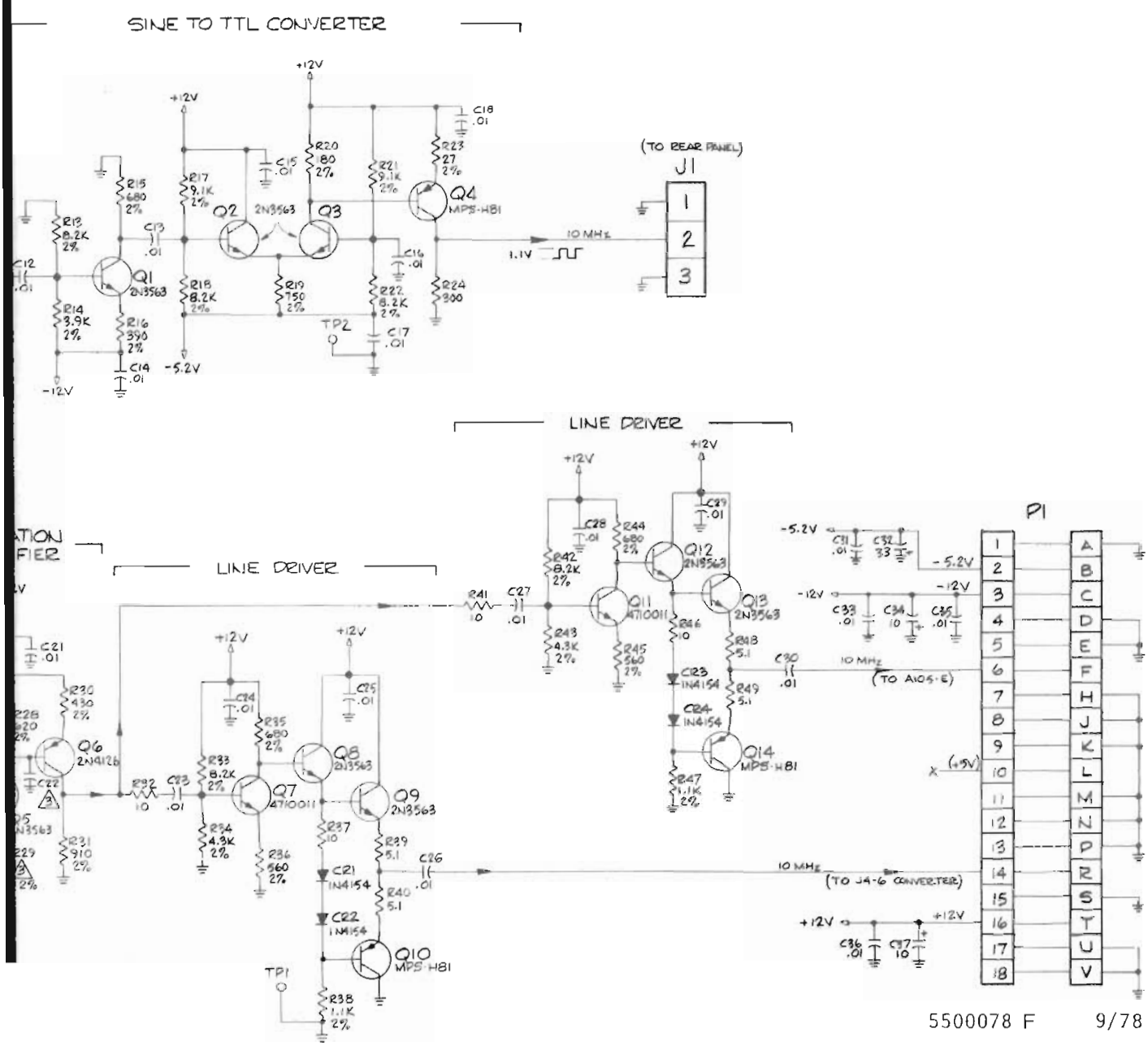
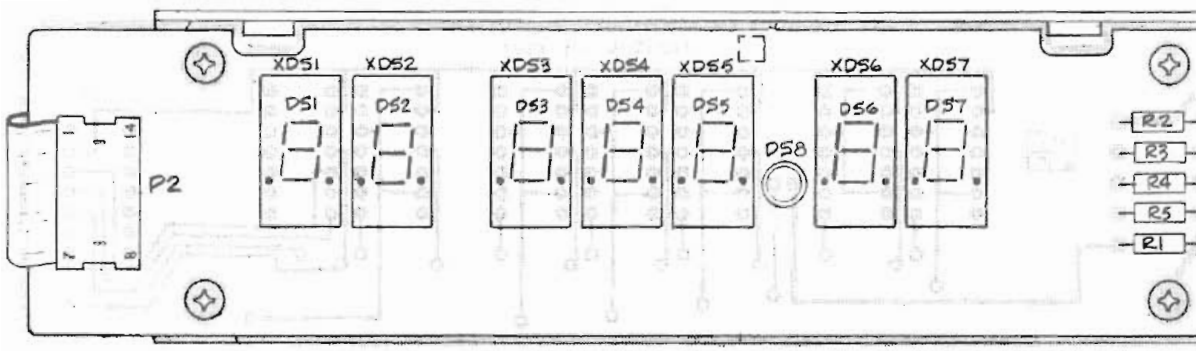


FIGURE 9-10B
SCHEMATIC DIAGRAM
REFERENCE OSCILLATOR BUFFER (A108)


XDS1
XDS2
XDS3
XDS4
XDS5
XDS6
XDS7
DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
P2
R2
R3
R4
R5
R1

080C

DISPLAY (A110)

Display board A110 contains seven LED numerical display units mounted side-by-side, grouped into a 2-digit GHz section, and a 5-digit MHz section. The MHz section also contains an LED decimal point between the second and third least-significant digits (decimal point extinguishes when the two least-significant-digits are blanked by the front panel RESOLUTION switches). All drive signals for the display are obtained from the Count Chain Control.

The digit displays are 7-segment LED's, with the anodes of all segments of each digit tied together. When the anode is at a positive voltage, grounding any cathode through its associated resistor illuminates that segment.

In this multiplexed system, the anode supply voltage is applied in pulses (through anode drivers), which are synchronized with the cathode data to determine which segment shall light. The segment drive is applied directly to all display digits. Corresponding cathode segments are all tied together in groups of seven.

The LED digits each use a single transistor driver. The drivers saturate when turned on, applying a voltage almost equal to the supply voltage for the display. This voltage is variable (by A102R35) for display brightness adjustment.

Four display lamps are included on this assembly, which illuminate to indicate GATE operation, input signal LEVEL, LOCK, and REMOTE operation (Option P4).

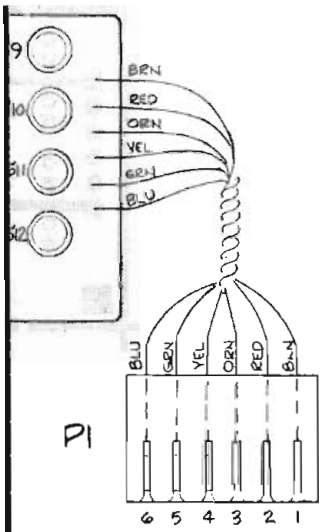
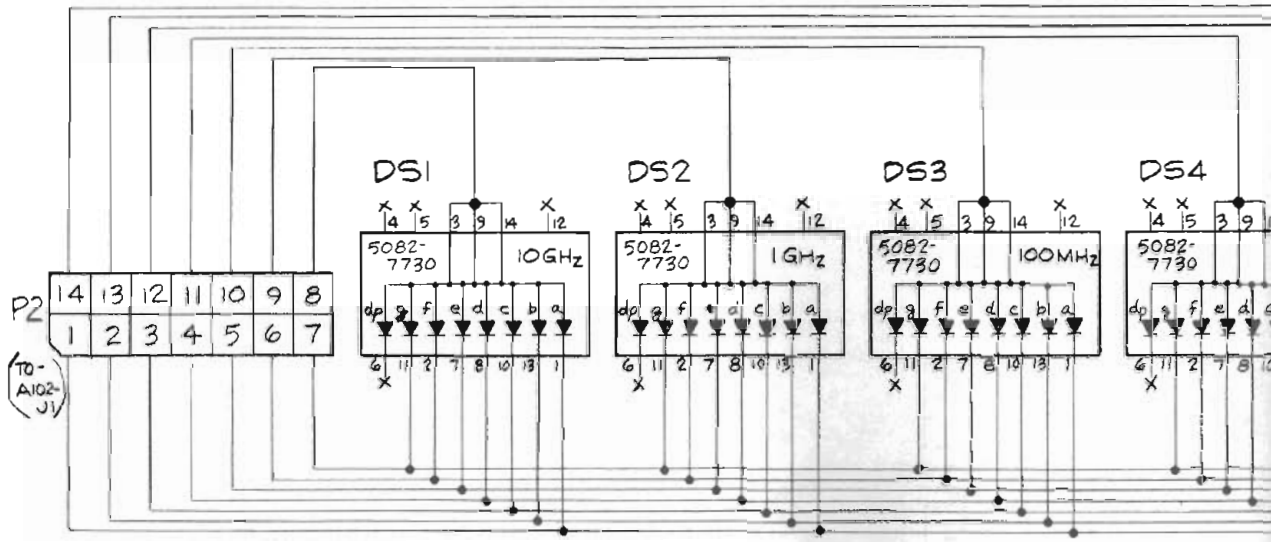
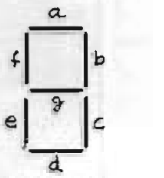
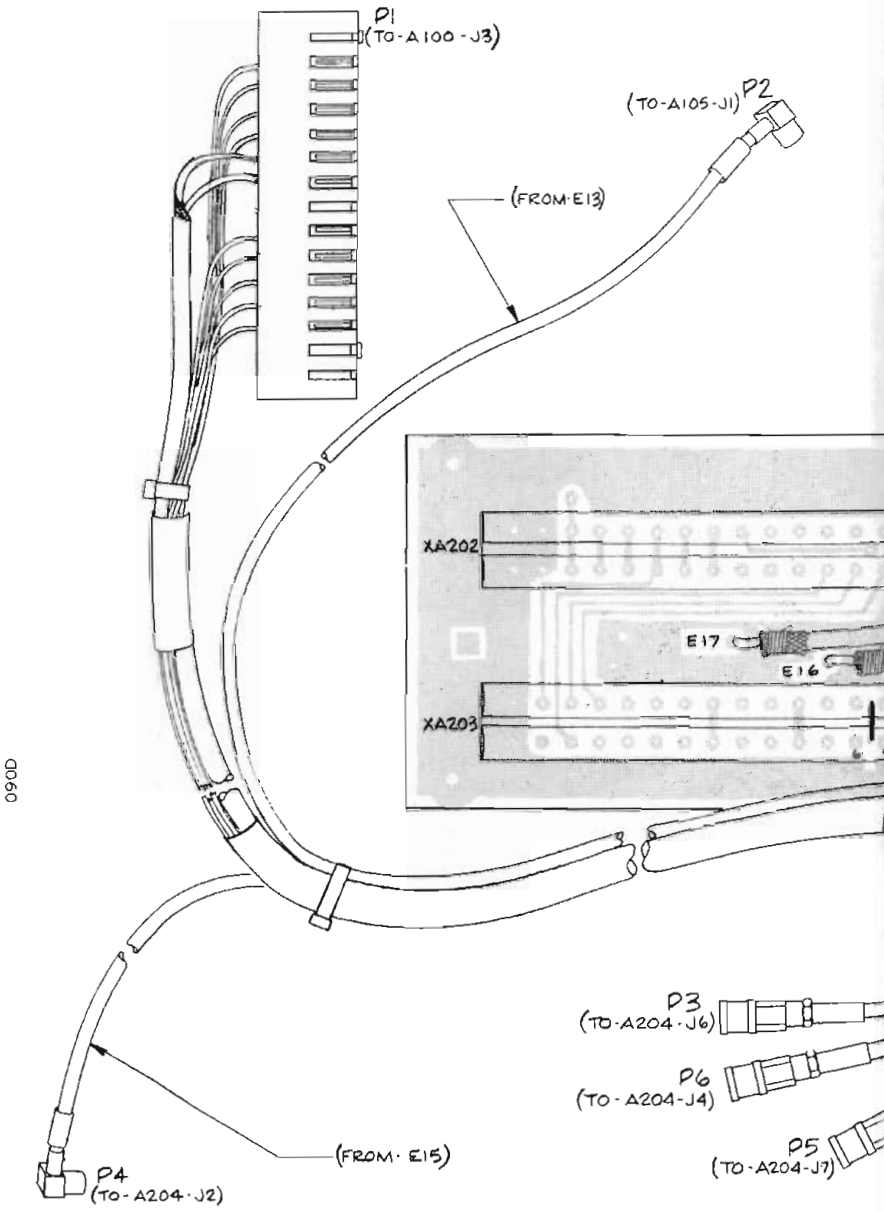


FIGURE 9-11A
COMPONENT LOCATOR
DISPLAY (A110)

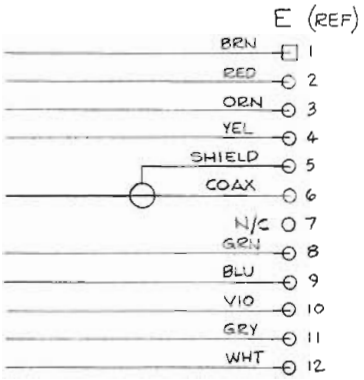

DS1
DS2
DS3
DS4
5082-7730
10GHz
1GHz
100MHz
P2
14 13 12 11 10 9 8
1 2 3 4 5 6 7
TO-A102-J1
dp g f e d c b a


a
f
b
g
e
c
d

DS1-DS7 KEY


P1
(TO-A100-J3)
P2
(TO-A105-J1)
(FROM-E13)
XA202
E17
E16
XA203
P3
(TO-A204-J6)
P6
(TO-A204-J4)
P5
(TO-A204-J7)
(FROM-E15)
P4
(TO-A204-J2)

090D



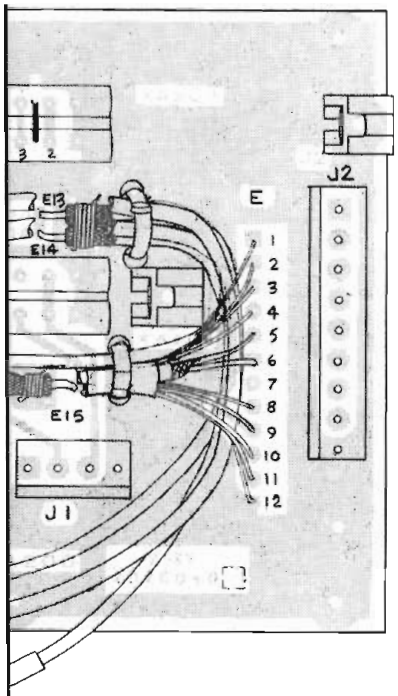
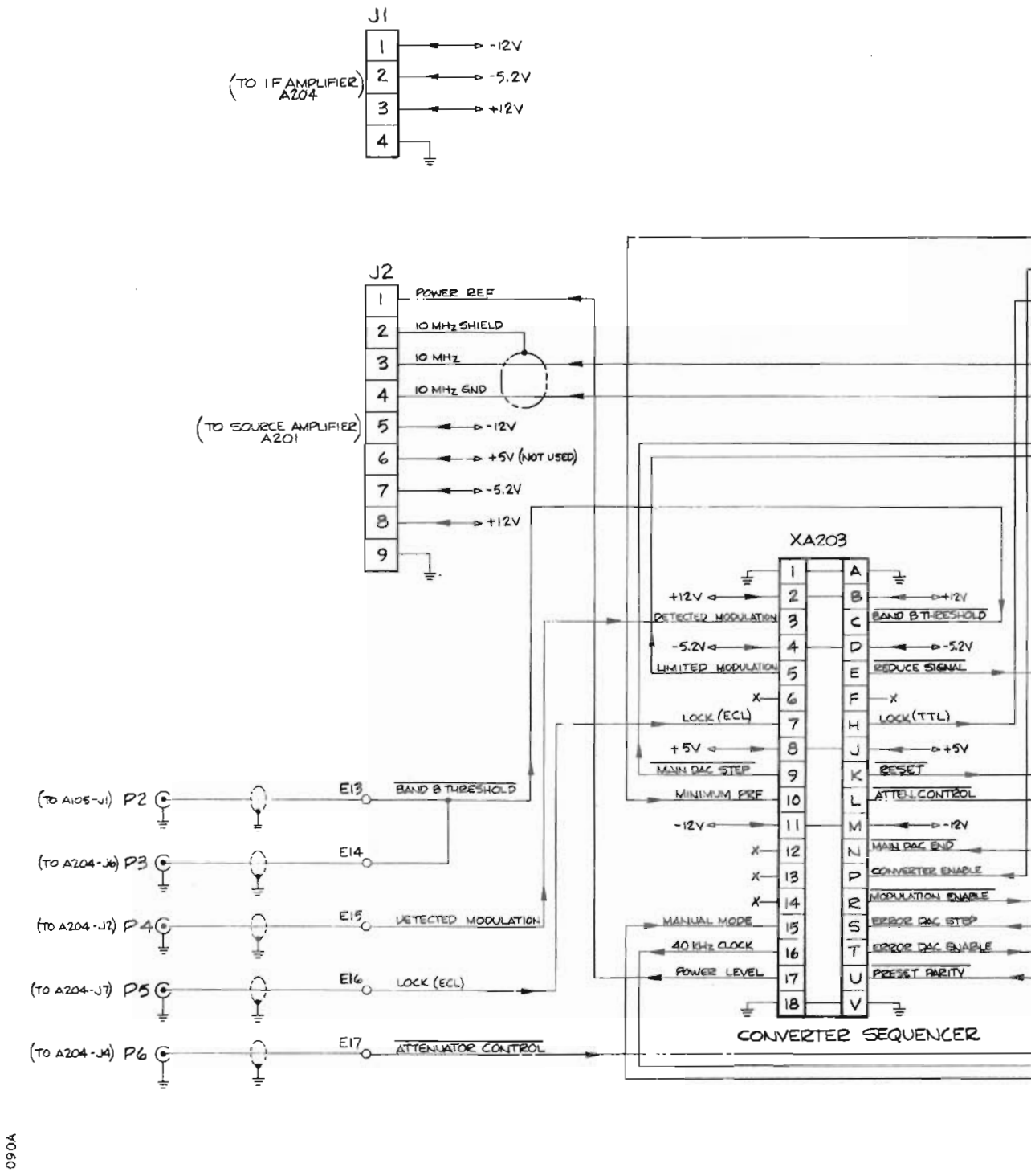


FIGURE 9-12A
COMPONENT LOCATOR
CONVERTER INTERCONNECT (A200)


J1
(TO IF AMPLIFIER A204)
1
2
3
4
-12V
-5.2V
+12V
J2
(TO SOURCE AMPLIFIER A201)
1 POWER REF
2 10 MHz SHIELD
3 10 MHz
4 10 MHz GND
5 -12V
6 +5V (NOT USED)
7 -5.2V
8 +12V
9
XA203
+12V
DETECTED MODULATION
-5.2V
LIMITED MODULATION
X
LOCK (ECL)
+5V
MAIN DAC STEP
MINIMUM PRF
-12V
X
X
X
MANUAL MODE
40 kHz CLOCK
POWER LEVEL
BAND B THRESHOLD
-5.2V
REDUCE SIGNAL
X
LOCK (TTL)
+5V
RESET
ATTEN CONTROL
-12V
MAIN DAC END
CONVERTER ENABLE
MODULATION ENABLE
ERROR DAC STEP
ERROR DAC ENABLE
PRESET PARITY
CONVERTER SEQUENCER
(TO A105-J1) P2
(TO A204-J6) P3
(TO A204-J2) P4
(TO A204-J7) P5
(TO A204-J4) P6
E13 BAND B THRESHOLD
E14
E15 DETECTED MODULATION
E16 LOCK (ECL)
E17 ATTENUATOR CONTROL

090A

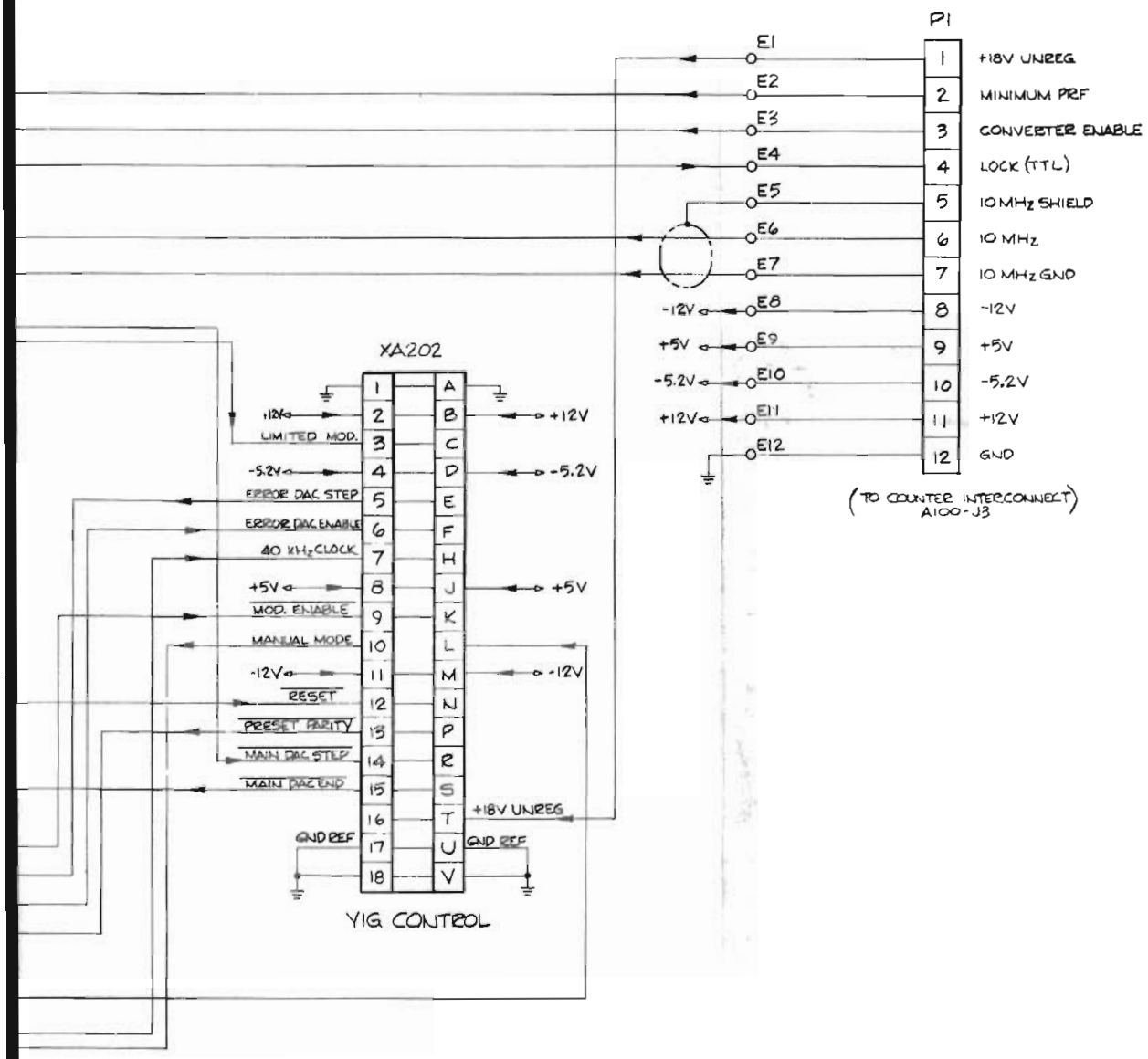
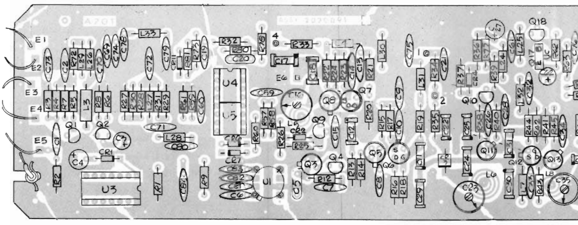
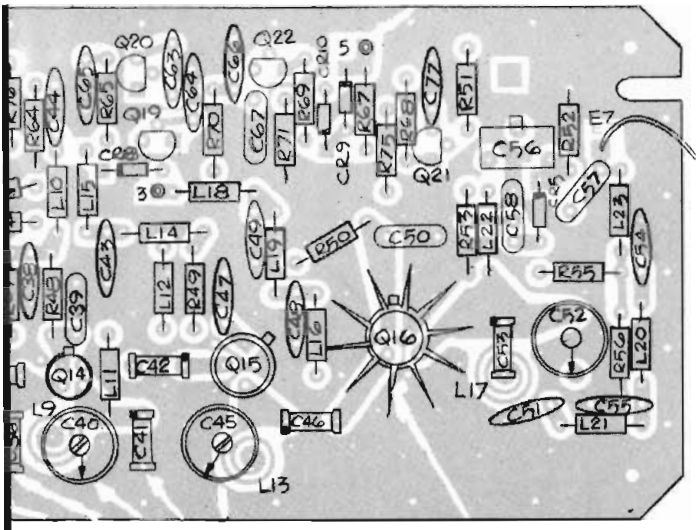


FIGURE 9-12B
SCHEMATIC DIAGRAM
CONVERTER INTERCONNECT (A200)



E1
E2
E3
E4
E5
U1
U3
U4
U5
Q1
Q2
Q3
Q4
Q5
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q18
CR1
C4
C71
L28
R32
R33
C17
L5
L6
L8
C35
R12
R26
R60



2020091 U
9/78

SOURCE AMPLIFIER (A201)

General

A source of up to one watt of power at 200 MHz is required to drive the step recovery diode Comb Generator in YIG Assembly A207. The 200 MHz must be both stable and coherent with the master oscillator in the counter. Stability is required to provide an IF spectrum that is dependent only upon the input signal spectrum. Coherence with the master oscillator is required to make counting accuracy dependent only upon the accuracy of the master oscillator.

The requirements of stability and coherence are satisfied by using a phase locked loop to lock a 200 MHz LC oscillator to the 10 MHz time base oscillator. The required output power is generated by a Class C amplifier that contains a leveling loop to set the power output at any desired level from 1 mW to 1.1 W.

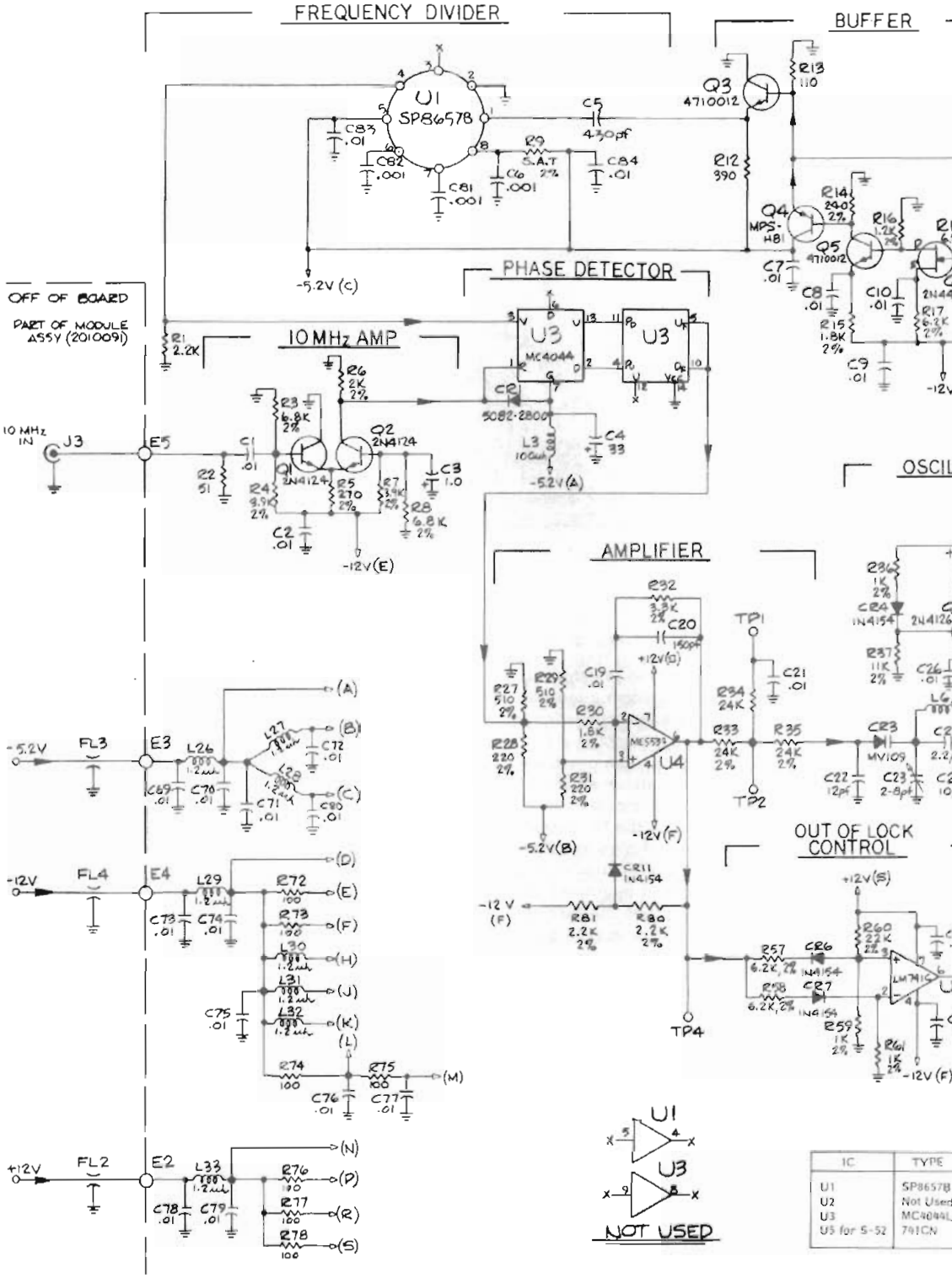
Circuit Description

The phase lock loop is a standard second order loop, implemented by using digital phase lock loop components. The 200 MHz LC oscillator is a modified Colpitts circuit with bias stabilization supplied by Q10. The output frequency of the 200 MHz oscillator is divided by 20 in U1 and U2 to produce a 10 MHz square wave. This signal is compared to the processed 10 MHz reference by phase detector U3. Phase error is amplified by active filter U4,and applied to voltage variable capacitor CR3. This holds the 200 MHz oscillator "locked" in phase to the 10 MHz reference signal. C23 sets the open loop center frequency of the oscillator.

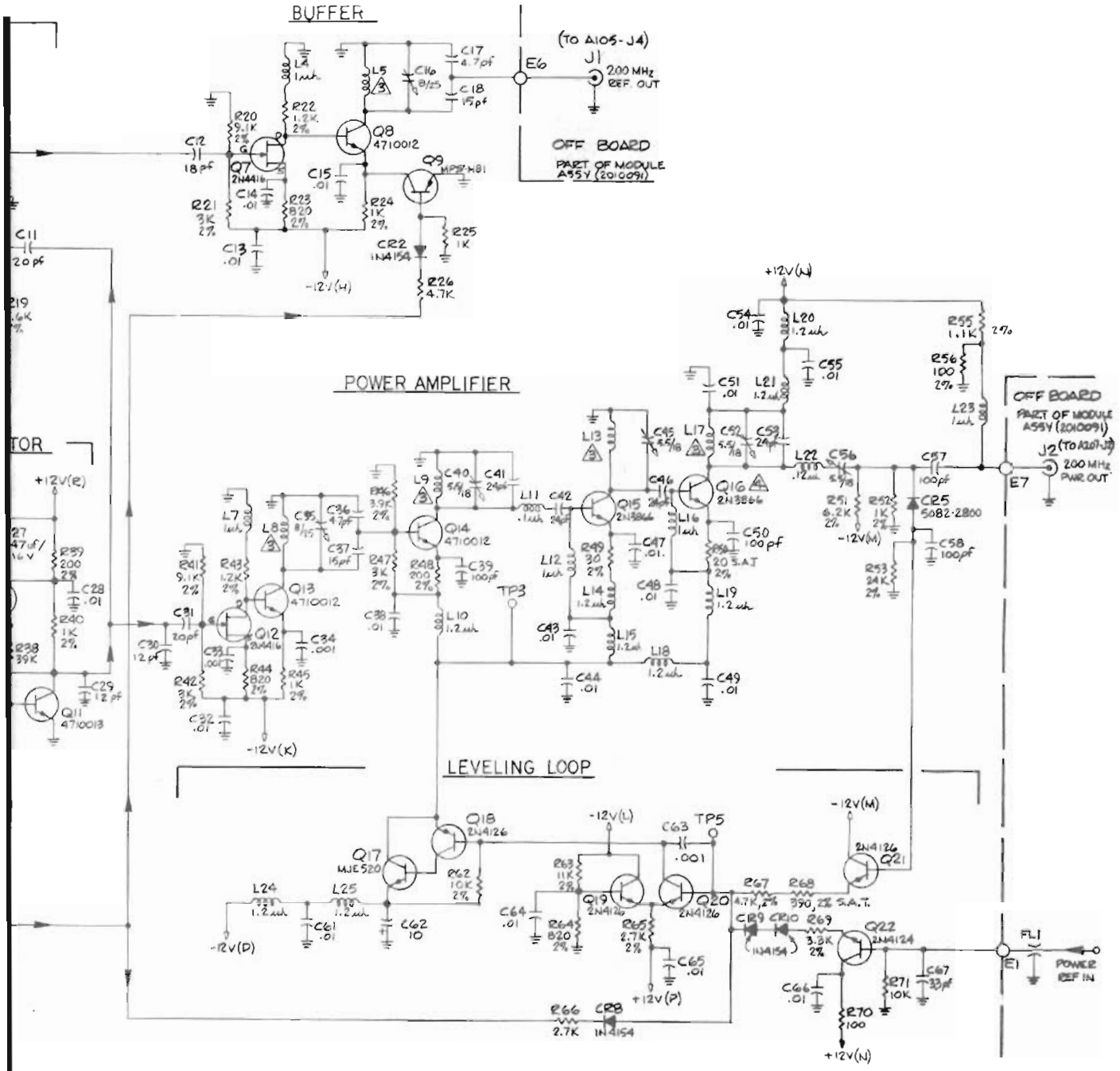
The main power amplifier consists of four stages: buffer amplifier Q12 and Q13, linear amplifier Q14, and two Class C stages Q15 and Q16. Output power level is controlled by adjusting the value of the negative voltage supplied by Q17 and Q18 to the linear amplifier and Class C stages.

The power leveling loop operates by sampling the peak value of the output signal with CR5, and comparing this peak value to the Power Reference. The comparison is made by differential amplifier Q19 and Q20, which in turn controls Q17 and Q18.

FIGURE 9-13A
COMPONENT LOCATOR
SOURCE/AMPLIFIER (A201)



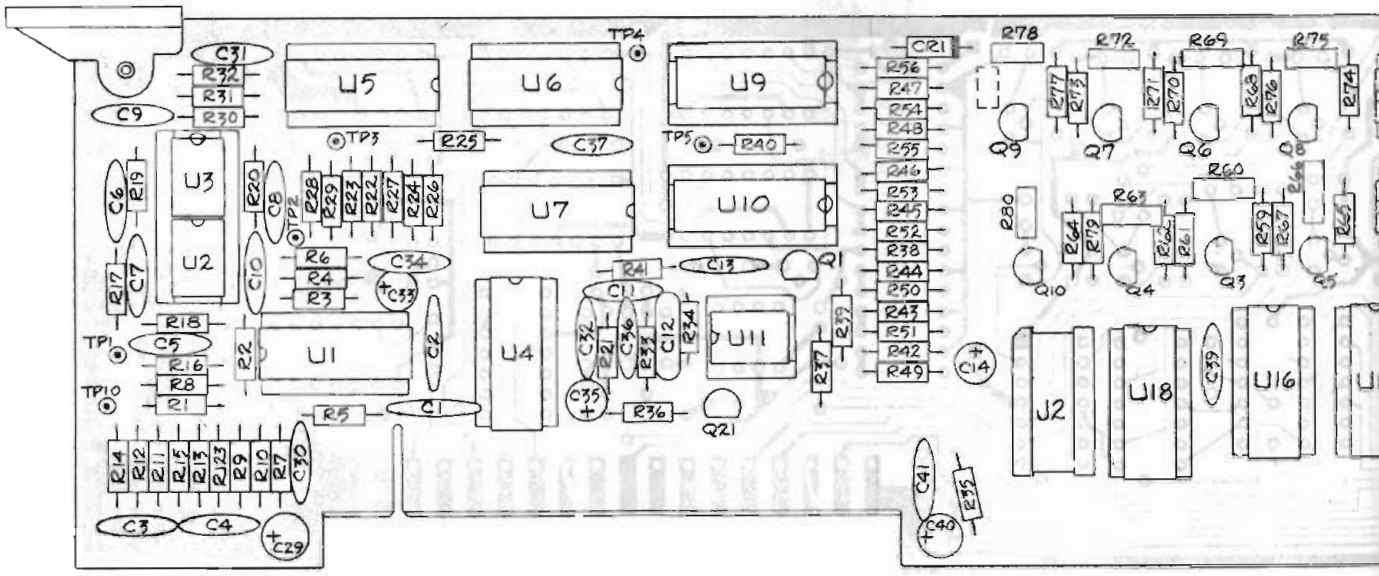
IC	TYPE
U1	SP8657B
U2	Not Used
U3	MC4044L
U5 for S-52	741CN



5500091 L 9/78

3 PART OF PC BOARD.

FIGURE 9-13B
SCHEMATIC DIAGRAM
SOURCE/AMPLIFIER (A201)



YIG CONTROL (A202)

General

The YIG Control Board (A202) contains circuits required to set the frequency of the YIG filter (A207) and to generate the BCD preset information for the Count Chain (A103). The main digital-to-analog converter (DAC) selects a particular comb line and provides the output frequency information. An error DAC provides a correction signal to precisely center the YIG filter passband on a comb line, based on information derived from the centering circuits. These circuits operate by modulating the center frequency of the YIG passband at a 20 kHz rate. This causes the filter to be tuned back and forth through the desired comb line, producing a pulse each time the YIG passes through the comb frequency. The phase of this detected modulation is then compared to the modulation frequency to produce the required centering information.

Main DAC

Steps of 200 MHz to the YIG filter are controlled by the main DAC. This DAC consists of a voltage reference (CR3, U12), presettable BCD counters (U19, U20), a series of transistor switches (Q3-Q10), precision summing resistors, and a summing amplifier (U13). Data from the front panel thumbwheel switch is preset into U19 and U20 during the Reset period. Each output line controls a transistor switch which connects a precision resistor to the 3.1V voltage reference. The value of the resistor determines the current into the SUM line, while the summing amplifier provides a voltage output proportional to the total input current. The digital output of U19 and U20 are also used to provide 3MSD preset information to A103.

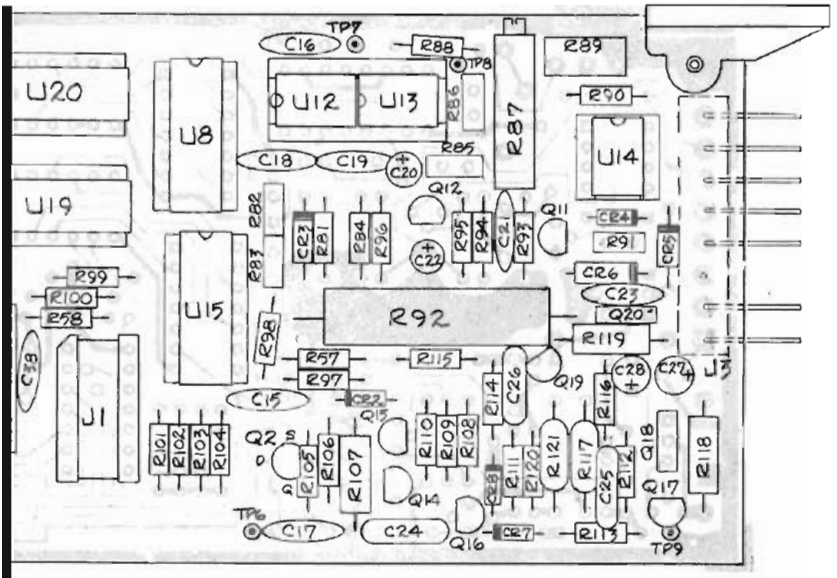
In the AUTO mode, pulses from A203 into the clock input of U19 cause the DAC to step in 200 MHz increments upon command. In the MANUAL mode, a Parity Checker (U16, U17, U18), compares the thumbwheel information with the actual states of U19 and U20. If they differ, an output is obtained which triggers a Reset, and in turn causes the DAC output to equal the thumbwheel switch setting.

YIG Driver

The voltage output of the summing amplifier is converted into a current in the YIG Driver (U14, Q11, Q12, and chassis mounted A2Q1). R89 sets the current offset, while R87 sets the slope. The current sense resistor (R92) provides the required feedback voltage for the driver. CR5 limits the voltage across the YIG filter tuning coil during Reset in order to protect Q12 and A2Q1.

YIG Passband Modulation

As part of the centering function, the center frequency of the YIG passband is modulated by means of an auxiliary tuning coil within the YIG. A 40 kHz clock is divided in U4 to produce a 20 kHz square wave. This signal is converted to a triangular waveform by integrator U11. This output is then converted to a current in the Modulation Coil Driver. Q14-Q16 form a high gain voltage amplifier. The single ended output at the collector of Q16 is converted to a bipolar output with Q17 and Q19, while CR7 and CR8 compensate for base emitter junction voltages. Q18 and Q20 provide increased current capability. Feedback for the driver is supplied by sensing the current through R107, thus converting the voltage input to a current output. Nominal deviation of the YIG center frequency is ± 50 MHz.



2020092 P
9/78

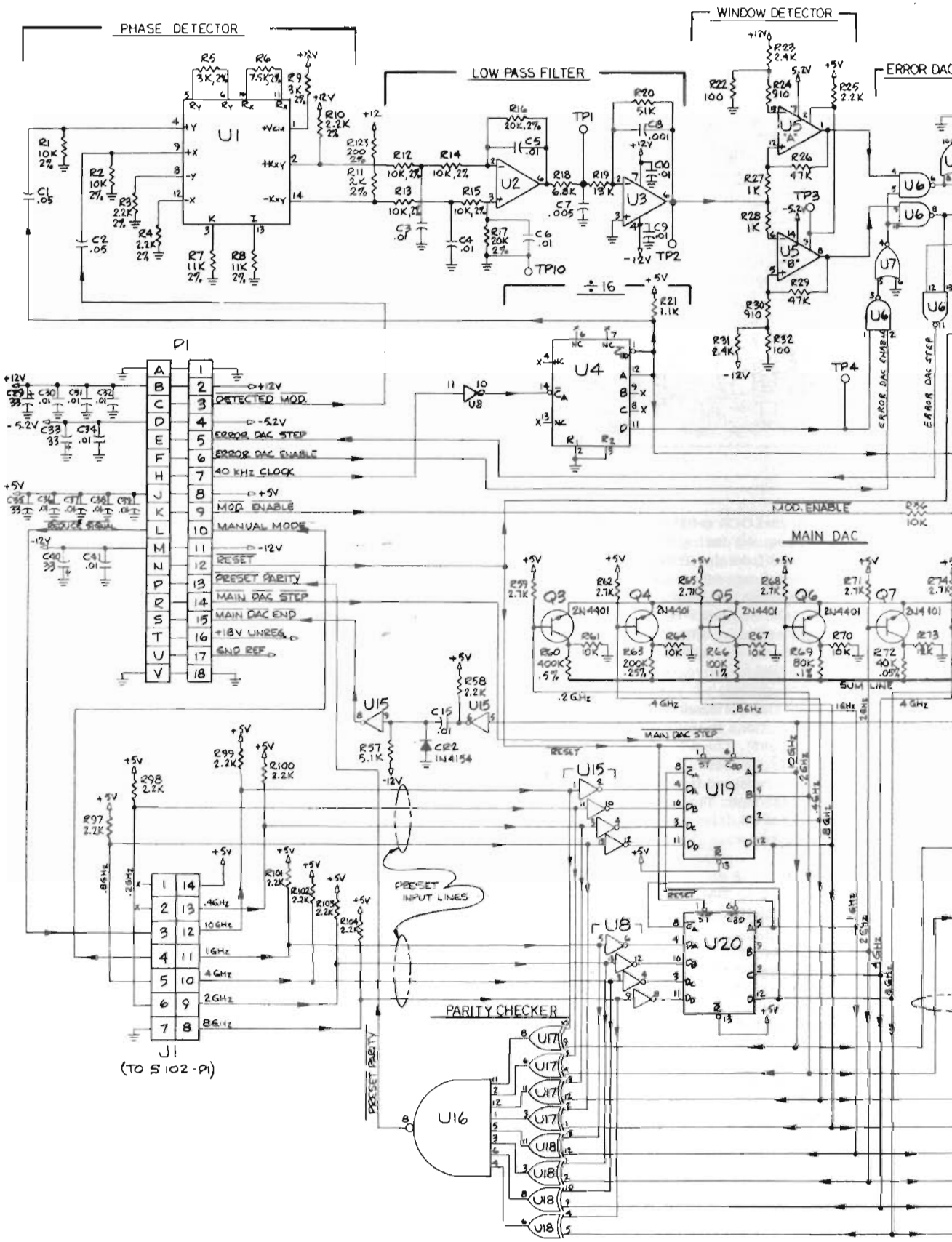
YIG Centering Circuit

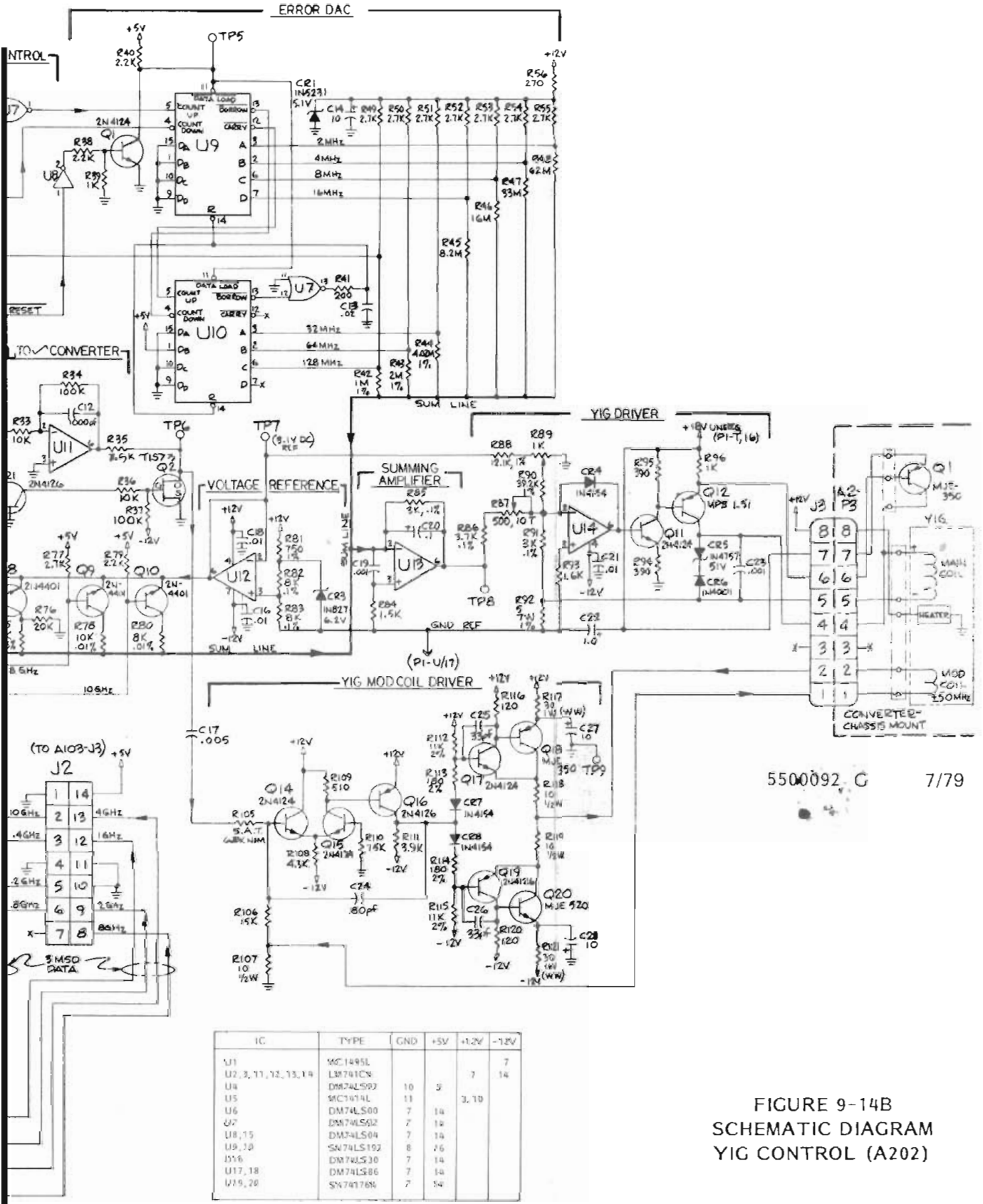
Centering of the YIG passband is achieved by detecting the output of the modulated comb generator and phase comparing it to the modulation frequency in U1. U1 is a four quadrant multiplier, producing outputs proportional to the product of two inputs. The positive and negative outputs of U1 differentially drive an active low pass filter (U2), which in turn, drives another low pass filter (U3). The output of U3 represents the DC component of the output of U1. Its amplitude and sign are directly related to the frequency offset of the YIG filter passband from the comb frequency. This signal is sensed by window detector U5. If the output at U3 exceeds the threshold reference, one of the two outputs of U5 is driven high.

The two outputs of U5 are used to control the Error DAC. This DAC supplies an error signal directly into the Main DAC summing amplifier. R42-R48 are summing resistors switched on by U9 and U10 (binary up-down counters). Clock pulses from U4 at a 2.5 kHz rate cause U9 to either count up, count down, or remain fixed depending on the outputs of U5.

Thus, a continually increasing (or decreasing) error signal is applied to the main tuning coil of the YIG until the DC output of U3 falls inside the threshold limits. The Borrow output of U10 provides a low level clamp on the DAC, while the C output of U10 provides a high level clamp. The Error DAC step at U6 pin 11 provides the information to the Converter Sequencer (A203) that the YIG centering cycle is completed.

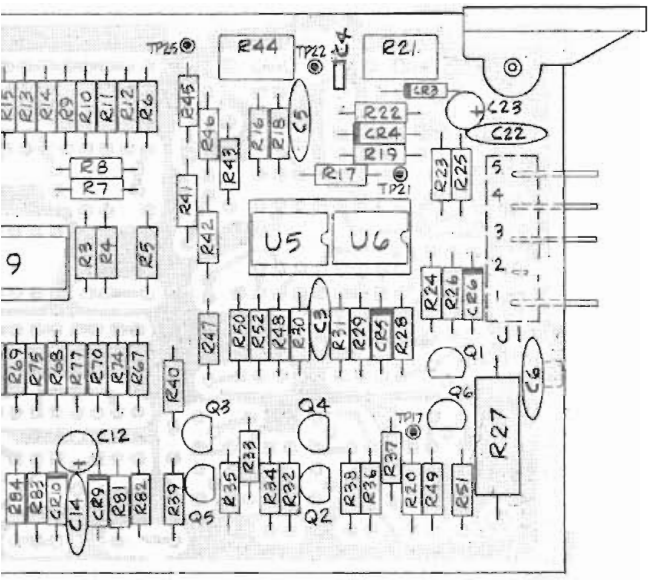
FIGURE 9-14A
COMPONENT LOCATOR
YIG CONTROL (A202)


PHASE DETECTOR
LOW PASS FILTER
WINDOW DETECTOR
ERROR DAC
÷16
MAIN DAC
PARITY CHECKER
P1
J1
(TO S-102-P1)
U1
U2
U3
U4
U5
U6
U7
U8
U15
U16
U17
U18
U19
U20
Q3
Q4
Q5
Q6
Q7
2N4401
DETECTED MOD.
ERROR DAC STEP
ERROR DAC ENABLE
40 KHz CLOCK
MOD ENABLE
MANUAL MODE
RESET
PRESET PARITY
MAIN DAC STEP
MAIN DAC END
+18V UNREG
GND REF
PRESET INPUT LINES
SUM LINE
.2 GHz
.4 GHz
.86Hz
1GHz
2GHz
4GHz
TP1
TP2
TP3
TP4
TP10
CR2
IN4154



IC	TYPE	GND	+5V	+12V	-12V
U1	MC1495L				7
U2,3,11,13,15,14	LM741CN			7	14
U4	DM74LS93	10	5		
U5	MC10114L	11		3,10	
U6	DM74LS00	7	14		
U7	DM74LS02	7	14		
U8,15	DM74LS04	7	14		
U9,10	SN74LS193	8	16		
U16	DM74LS30	7	14		
U17,18	DM74LS86	7	14		
U19,20	SN74176N	7	14		

FIGURE 9-14B
SCHEMATIC DIAGRAM
YIG CONTROL (A202)



2020093 AA
9/78

Sequence 7 is the LOCK sensing portion of the sequence. If the signal received during Sequence 4 or 5 resulted in a LOCK command from the IF Processor, then the sequence will remain in Sequence 7, and send a LOCK command to the Control board (A104) in the Basic Counter. If no LOCK was obtained, the Sequencer will continue to Sequence 0, and repeat the sequence with the next comb line.

Attenuator Control

The Attenuator Control circuits perform the function of limiting the variations in input signal amplitude as seen by the Mixer (A205). The ATTENUATOR CONTROL command from the IF Processor (A204) is activated whenever the input signal received by A205 exceeds the minimum signal by at least 7 dB. This command triggers one-shot U3. The output of U3 drives a DAC consisting of a counter (U4), summing resistors (R9 - R14), a summing amplifier (U5), and an inverting amplifier (U6). Each DAC step results in a nominal 0.5 dB increase in attenuator insertion loss. The REDUCE SIGNAL indicator on the front panel is activated when the DAC reaches its 32nd step.

The DAC acts as a sample and hold circuit for attenuation level. As long as there is insufficient attenuation, the ATTENUATOR CONTROL command will cause the attenuation to increase 0.5 dB for each input pulse. On long pulses or CW signals, U3 will retrigger as long as the ATTENUATOR CONTROL command remains active.

In addition to increasing attenuator insertion loss, the ATTENUATOR CONTROL command forces the Sequence Generator to Sequence 3 by activating the preset strobe line of U8. Since the RF switch remains open, and the YIG modulation is not enabled, the Sequencer then moves on through Sequence 4 and 5, and again waits for Band B Threshold. The result is that the Sequencer cannot go on to Sequence 6 until the attenuator has reduced the input signal sufficiently.

Attenuator Driver

The output of U6 is a voltage corresponding to the desired attenuation. This signal is converted into two related currents by the Attenuator Driver. These currents: I_{total} and I_{series}, determine both the attenuation and the input VSWR of the PIN Diode Attenuator (part of A206).

Series current is generated by the network of U5 and Q6. R53 is the sense resistor for the current source. The nonlinear current output versus input level is achieved with a double breakpoint shaping network — Q2 and Q3 form one breakpoint, while Q4 and Q5 form the other. Variable resistor R47 sets the series current, and optimizes VSWR, at high attenuation levels.

Total current is the sum of series current and shunt current. The shunt current waveform is shaped by diode network CR2, CR3, and their associated resistors. Variable resistor R23 is used to adjust the ratio between series and shunt currents at moderate attenuation levels. U6 and current booster Q1, combine series and shunt networks to produce the total current output.

Power Level Control

During Sequence 1, the YIG comb level is set. This function is accomplished by varying the POWER REFERENCE level into the Source/Amplifier (A201). This in turn varies the 200 MHz power into the YIG/Comb Generator (A207). The comb line output is detected by the Mixer, and sensed by the Threshold Detector U17. Variable resistor R64 sets the threshold level.

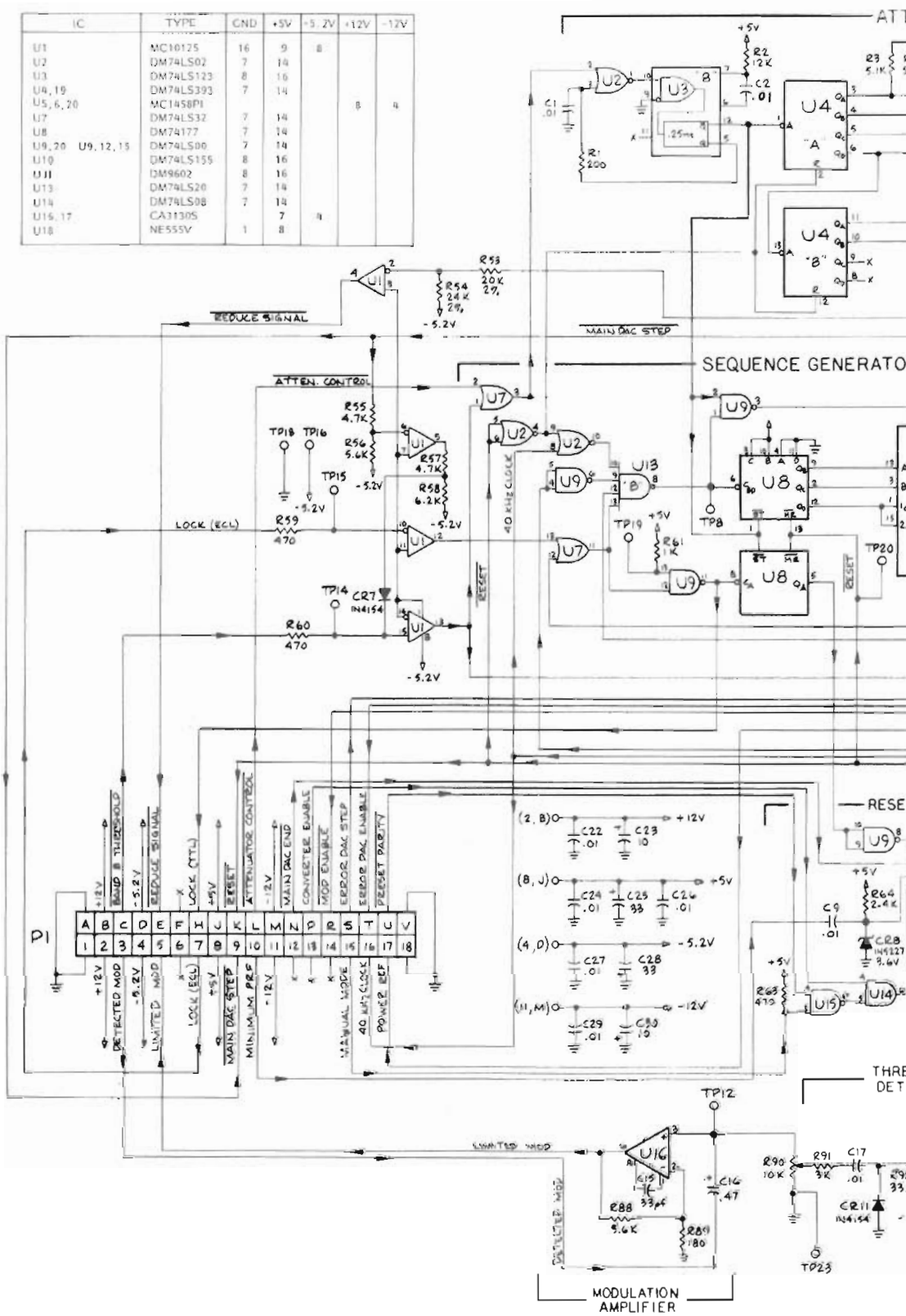
Operation of the Power Level Control begins at the end of the 1.5 ms period of U11. Clock pulses from U18 are then allowed to step the Power Level DAC (U19, R74 thru R80). When the comb output exceeds the threshold, U17 triggers, resetting the latch (U15 pin 10), inhibiting the clock input to the DAC and ending the sequence. If the DAC reaches maximum output, the same result is obtained.

FIGURE 9-15A
COMPONENT LOCATOR
CONVERTER SEQUENCER (A203)

SEQUENCE	FUNCTIONS	DURATION
0	1. Attenuator to max attenuation. 2. YIG Modulation enabled. 3. Main DAC step. 4. Reset state.	25 μs unless held by RESET.
1	1. YIG comb leveling cycle.	1.5 - 4.7 msec.
2	1. Initiate YIG centering cycle.	25 μ seconds.
3	1. YIG centering cycle.	1 - 10 mseconds.
4	1. Attenuator to normal control. 2. Modulation off. 3. Initiate wait for Band B Threshold.	25 μ seconds.
5	1. Wait for Band B Threshold.	Depends upon PRF.
6	1. 25 μ second delay.	25 μ seconds.
7	1. LOCK sensing sequence.	25 μ sec if no LOCK.

TABLE 9-15A. CONVERTER SEQUENCE FUNCTIONS

IC	TYPE	GND	+5V	+5.2V	+12V	-12V
U1	MC10125	16	9	8		
U2	DM74LS02	7	14			
U3	DM74LS123	8	16			
U4,19	DM74LS393	7	14			
U5,6,20	MC1458PI				8	4
U7	DM74LS32	7	14			
U8	DM74177	7	14			
U9,20 U9,12,15	DM74LS00	7	14			
U10	DM74LS155	8	16			
U11	DM9602	8	16			
U13	DM74LS20	7	14			
U14	DM74LS08	7	14			
U16,17	CA3130S		7	4		
U18	NE555V	1	8			



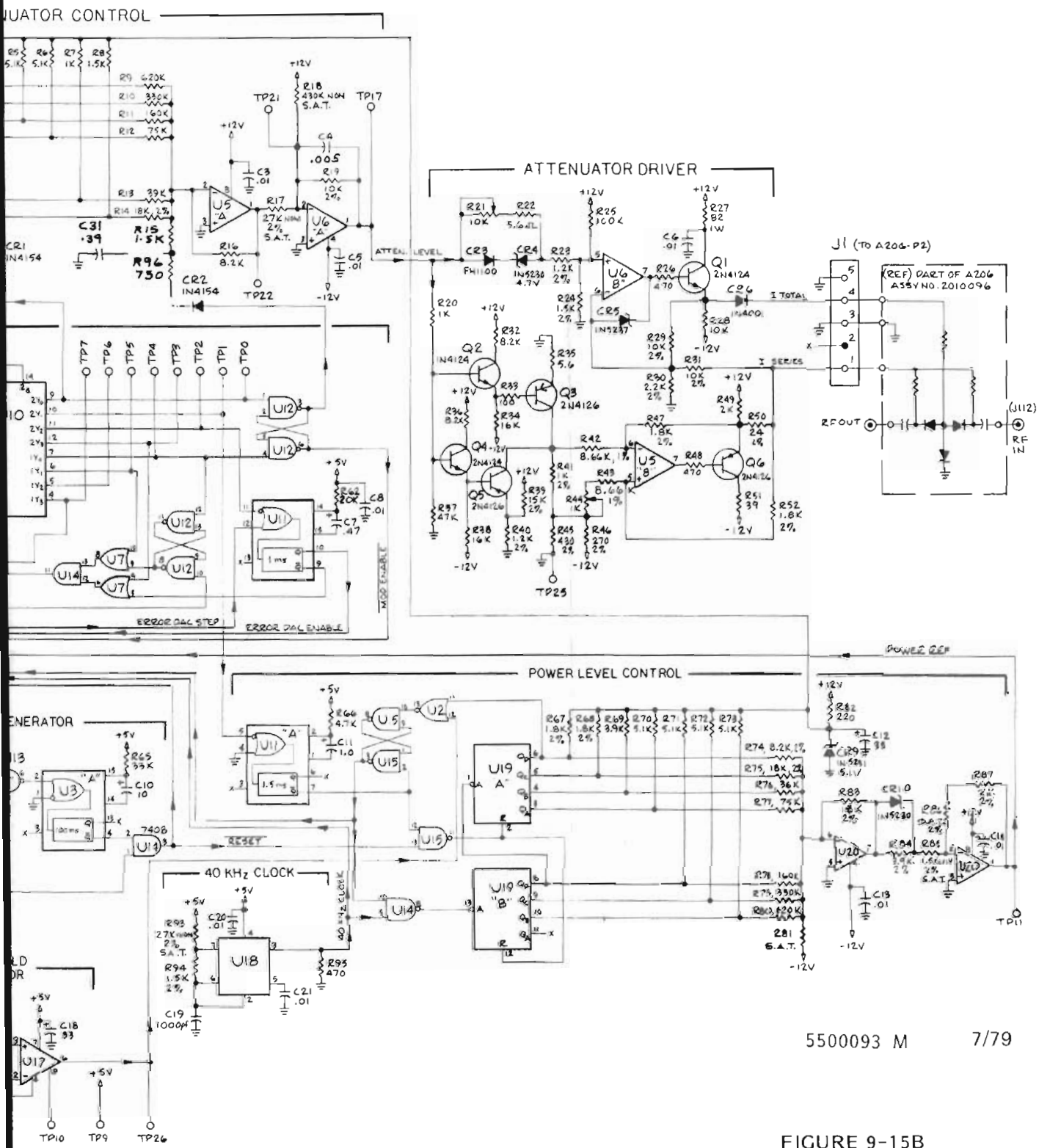
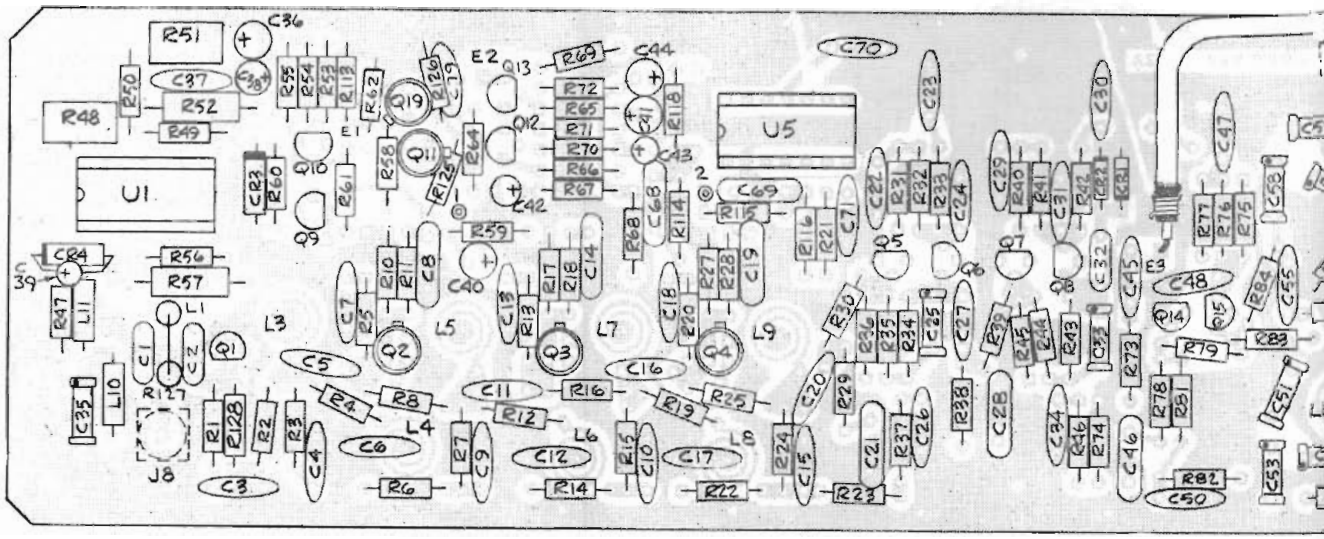


FIGURE 9-15B
SCHEMATIC DIAGRAM
CONVERTER SEQUENCER (A203)



IF PROCESSOR (A204)

IF Processor A204 receives its input from the Mixer (A205). It separates the Mixer output into IF and Video components, and processes the components to produce several outputs. The IF signal is amplified and limited for counting. The Video signal is used to produce the SIGNAL THRESHOLD, DETECTED MODULATION, and ATTENUATOR CONTROL signals directly. SIGNAL THRESHOLD is combined with the external INHIBIT INPUT to produce BAND B THRESHOLD. This signal, together with the IF signal, is used to determine LOCK.

IF Amplifier

The IF component of the Mixer output is amplified in a six stage amplifier having an overall gain of 50 dB, and a bandwidth covering 100 MHz to 375 MHz. Stage 1 (Q1) is a common emitter amplifier with shunt feedback (R2). L2 and L3 provide high frequency shaping of the response. Stages 2, 3, and 4 (Q2-4) are similar to Stage 1. Gain is set by the emitter resistors. High frequency gain shaping is provided by the emitter RC network (R11,C8), and the collector inductor (L5).

Stages 5 and 6 are limiting amplifiers, each consisting of an amplifier (Q5,Q7) and an emitter follower (Q6,Q8). Each stage has a nominal gain of 10 dB, determined by the input and feedback resistors (R30,34,35). Capacitive bypassing (C25) is used for high frequency gain shaping. Diodes (CR1,2) limit the final output still further.

Video Circuits

The Video output of the Mixer, representing the detected envelope of a microwave signal, is amplified by U1. R48 sets the voltage gain (nominally 100), while R51 nulls out any offset between the differential outputs at U1 pins 7 and 8.

Outputs of U1 are applied to a high speed differential amplifier (Q9,10). Positive feedback from R61 converts this circuit to a Schmitt trigger. Q11 is an emitter follower used to drive the high speed ECL gates. The same outputs of U1 also differentially drive comparator U5 which forms the Attenuator Threshold Detector. Resistive biasing and feedback (R114-116,118) set the trigger level of this circuit approximately 7dB above the Signal Threshold Detector level.

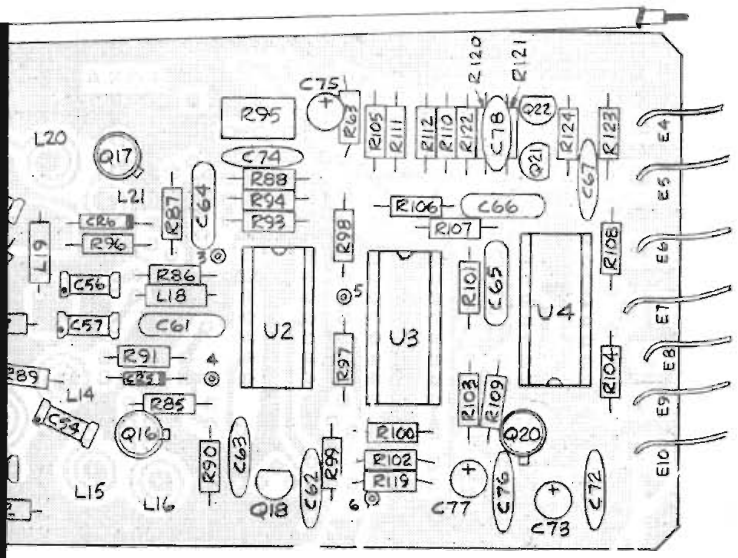
The remaining Video circuit is the 20 kHz amplifier consisting of Q12 and Q13. This circuit provides an additional voltage gain of 100 at frequencies near 20 kHz, and is used to detect the modulated comb lines during YIG leveling and centering operations.

In-Band Detector

The In-Band Detector determines whether or not an IF signal exists within the correct frequency range and at sufficient level to obtain LOCK. The correct frequency range is the region from 100 MHz to 325 MHz. After LOCK, the upper end of this region is extended to 350 MHz.

A portion of the IF signal is coupled into an additional limiter section (Q14,15) similar to the limiters in the IF Amplifier section. The output then drives two filter networks in parallel. The output of each network is detected (CR5,-CR6), and compared in U2. Since input signal amplitude is held constant, the detected signals are determined entirely by the filter characteristics. One of the filter networks consists of a 100 MHz high-pass section (C51-53,-L12) in series with a 325 MHz low-pass section (L13-16,-C54), thus forming a band-pass filter from 100-300 MHz.

The second network consists of a 100 MHz low-pass section (L17-19,C57) in parallel with a 325 MHz high-pass section (C58-60,L20,L21), forming a band reject filter from 100-325 MHz.



2020094 N
9/78

By comparing the outputs of these two networks in U2, a determination of the IF frequency is made. R95 is used to precisely set the crossover frequency. After LOCK is obtained, Q16 and Q17 are turned on, shorting out L16 and L21, and increasing the crossover point from 325 MHz to 350 MHz.

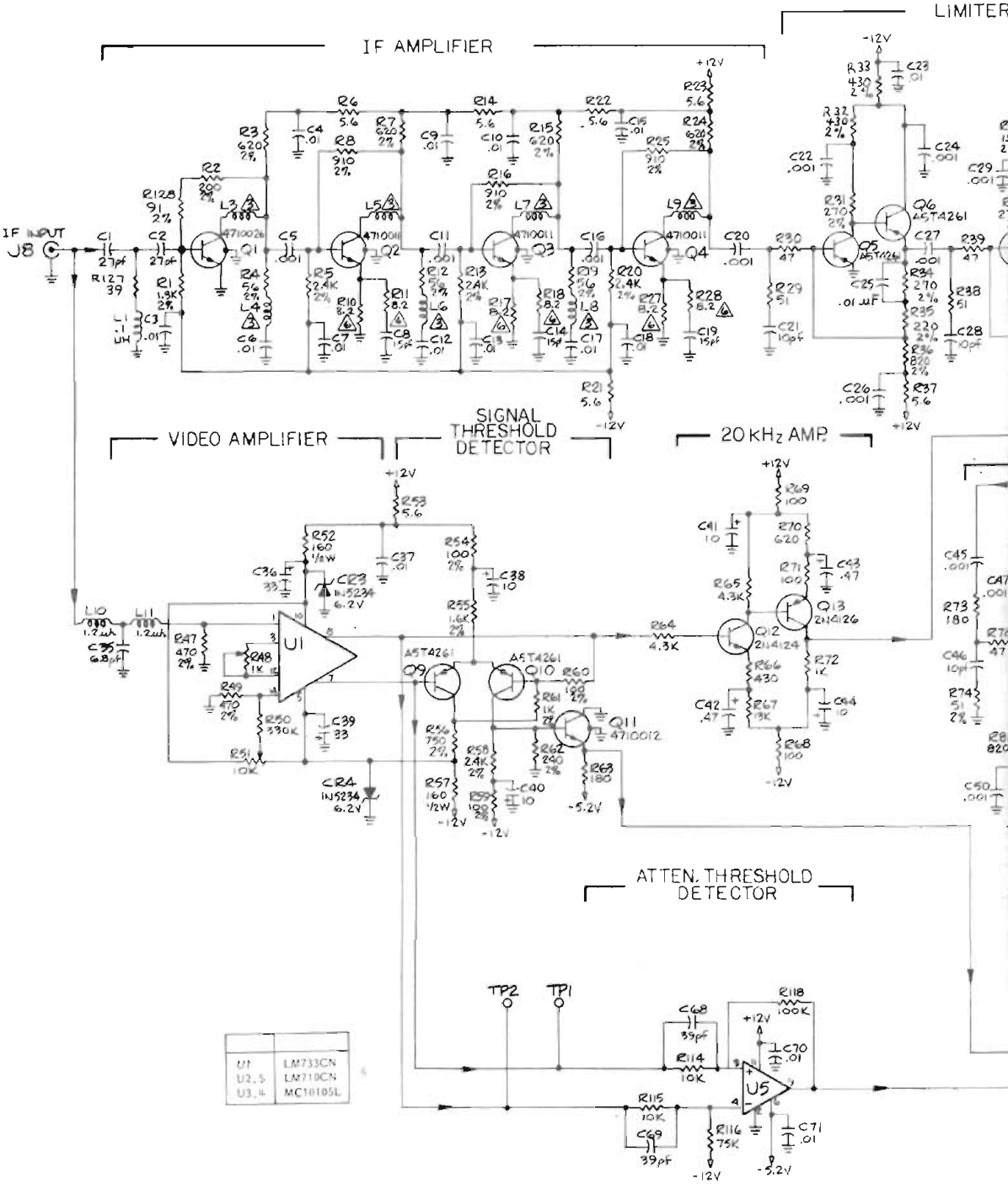
LOCK Logic

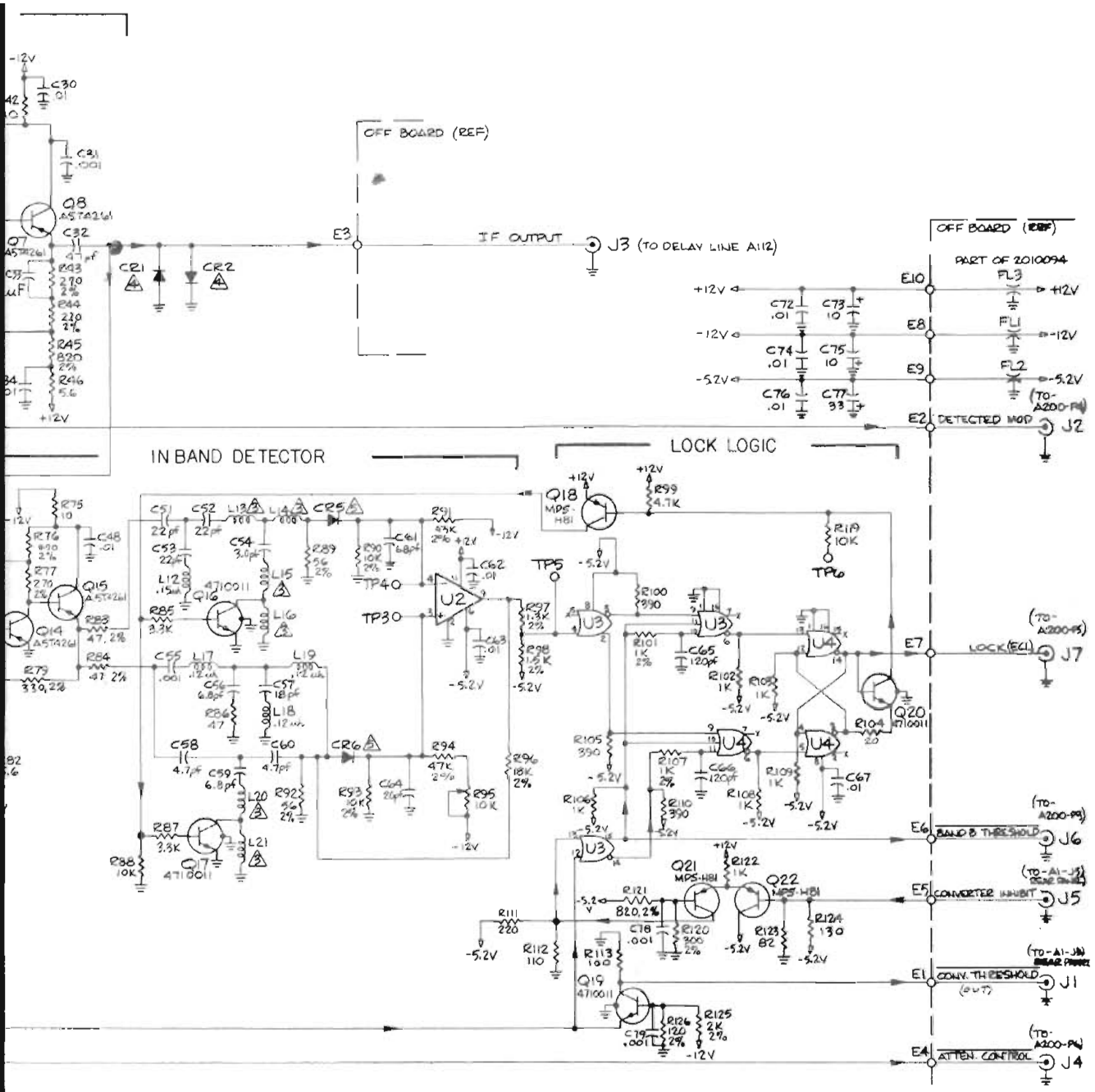
The LOCK logic determines whether or not the proper conditions exist to consider the Converter locked. The condition to obtain LOCK is that an In-Band signal (from U2 pin 9) appears within 70 nanoseconds of the appearance of BAND B THRESHOLD (at Q11 collector). Once this condition is met, the LOCK command is latched, and remains active until a loss-of-lock condition is obtained — that is: an In-Band signal is not received within 70 nanoseconds of BAND B THRESHOLD.

BAND B THRESHOLD is generated by combining CONVERTER THRESHOLD (from Q11) with the external INHIBIT INPUT. The INHIBIT INPUT is buffered by Q21 and Q22. The two signals are combined at pins 12 and 13 of OR gate U3.

The LOCK latch consists of two gates of U4 with the output at U4 pin 14. The set input to this latch (U4 pin 5) is driven by a 3-input NOR gate (U4). The latch is set when all three inputs of the NOR gate are simultaneously low. R107 and C66 provide a 70 nanasecond delayed BAND B THRESHOLD to one input, while the inverted signal without a delay is applied to the second input. An inverted IN-BAND signal is applied to the third input. Thus a 70 nanosecond interval exists after BAND B THRESHOLD occurs, during which the LOCK latch may be set. The reset input to the latch is also a 3-input gate (U3), connected so IN-BAND must occur within 70 nanoseconds or the latch will be reset. If IN-BAND drops out while BAND B THRESHOLD remains (at any point in time after the 70 nanosecond interval), the latch is immediately reset.

FIGURE 9-16A
COMPONENT LOCATOR
IF PROCESSOR (A204)


LIMITER
IF AMPLIFIER
VIDEO AMPLIFIER
SIGNAL THRESHOLD DETECTOR
20 kHz AMP
ATTEN. THRESHOLD DETECTOR
IF INPUT
J8
+12V
-12V
-5.2V
U1
U5
Q1
Q2
Q3
Q4
Q5
Q6
Q9
Q10
Q11
Q12
Q13
CR23
CR24
IN5234
6.2V
TP1
TP2
U1 LM733CN
U2,5 LM710CN
U3,4 MC10105L



3 PART OF PC BOARD.

4 SEE PARTS LIST.

5 MATCHED PAIR.

5500094 J 7/79

FIGURE 9-16B
SCHEMATIC DIAGRAM
IF PROCESSOR (A204)

SECTION O

OPTIONS

O-1. This section provides schematic diagrams, circuit descriptions and component locators, for options available for use with the 451 Microwave Pulse Counter.

O-2. OPTION P1 - TCXO

O-3. For a description of the use of this option, refer to paragraphs 3-29 through 3-38, and paragraph 4-28. The TCXO is installed on Reference Oscillator Buffer board A108 in place of the standard RTO. See pages 9-20 and 9-21 for schematic, board layout, and circuit description.

O-4. OPTION P2 - PRESCALER

O-5. This option extends the frequency range of the 451 down to 300 MHz to 950 MHz. See pages O-2 and O-3 for schematic, board layout, and circuit description.

O-6. OPTION P3 - REAR PANEL INPUTS

O-7. For this option, the Converter is switched end-for-end, with the Band B input connector projecting through the existing opening in the rear panel, and with certain cables re-routed and changed in length.

O-8. TO FIELD CHANGE BAND B TO REAR INPUT

a. Disconnect power cord, and remove both top and bottom covers from the counter.

b. Unplug all cables which connect Converter to Basic Counter. Note cable routing and connections.

c. Unscrew Converter tray retaining screws (from bottom of Counter).

d. Lift rear of Converter tray, and carefully slide Converter out of counter enclosure.

e. Turn Converter end-for-end, and insert the Band B connector through the hole in the rear panel labeled 925 MHz - 18 GHz.

f. Lower Converter carefully into counter enclosure, taking precautions not to pinch any wires or cables.

g. Install screws which hold Converter in enclosure, and reconnect cables unplugged in step b above.

h. Perform Incoming Operational Check described in Section 2 - Installation.

i. Apply a signal to the Band B input connector within the correct frequency and power limits, checking for proper operation of the Converter. Specifications remain identical to those for front panel operation.

O-9. TO FIELD CHANGE BANDS A AND B TO REAR INPUT

a. Disconnect power cord, and remove both top and bottom covers from the counter.

b. Unplug all cables which connect Converter to Basic Counter. Note cable routing and connections.

c. Unscrew Converter tray retaining screws (from bottom of Counter).

d. Lift rear of Converter tray, and carefully slide Converter out of counter enclosure.

e. Turn Converter end-for-end, and insert the Band B connector through the hole in the rear panel labeled 925 MHz - 18 GHz.

f. Lower Converter carefully into counter enclosure, taking precautions not to snag or pinch any wires or cables.

g. Install screws which hold Converter in enclosure.

h. Locate Double Delay Line Assembly A116. Note that three cables exit from under one end of the cover, and one cable (to A204J3) exits from under the other end of the cover. Loosen, but do not remove the screws holding the Delay Line cover in place. Re-route the cable to A204J3 so it exits from the same end as the remaining three cables. Tighten the Delay Line cover screws.

i. All three plug-in cables to the Prescaler PC board (A109) must be replaced with those of a different length as follows: Replace short W30 cable (A109J1 - A1J111) with long W30 cable (with BNC connector mounted on rear panel); replace short W31 cable (A109J5 - A204J1) with long W31 cable; replace long W32 cable (A109J4 - A204J5) with short W32 cable.

j. Reconnect all cables unplugged in steps b and i.

k. Perform Incoming Operational Check described in Section 2 - Installation.

l. Apply a signal to the Band B input connector within the correct frequency and power limits, checking for proper operation of the Converter. Specifications remain identical to those for front panel input.

m. Apply a signal to the Band A input connector within the correct frequency and power limits, checking for proper operation of the Prescaler. Specifications remain identical to those for front panel input.

O-10. OPTION P4 - BCD OUTPUT/REMOTE PROGRAMMING

O-11. BCD output, remote programming, and YIG preset, are the three basic functions provided by this option. Circuitry to accomplish these functions is contained on PC board A111, with connections made through rear panel REMOTE INPUT/OUTPUT connector A1J7. All inputs and outputs are TTL compatible. Each basic function will be described separately, with A1J7 pin assignments and functions shown in Table O-1. (Recommended mating connector for A1J7: Amphenol 57-30500, 50 pin male — EIP Part No. 2640003.) See pages O-4 and O-5 for schematic and layout.

O-12. BCD OUTPUTS

O-13. BCD formated outputs to A1J7 correspond to the applied signal input frequency. A PRINT command output signal indicates the presence of valid data, while an INHIBIT input prevents the data from being altered. Both PRINT and INHIBIT signals are active high.

O-14. BCD information from High Frequency board A106 enters A111 via J5 and J6. U1 through U5 buffer the information and supply it via P1 to A1J7.

O-15. YIG PRESET

O-16. YIG preset information is supplied to the counter from two sources, depending upon the status of the Local/$\overline{\text{Remote}}$ line. In the Local mode, preset information comes from the front panel thumbwheel and MAN SELECT/AUTO SWEEP switches. In the $\overline{\text{Remote}}$ mode, preset information is obtained via A1J7, and controlled by the status of the Conv Man/$\overline{\text{Auto}}$ line. Increments of 200 MHz may be programmed using the standard 1-2-4-8 BCD code.

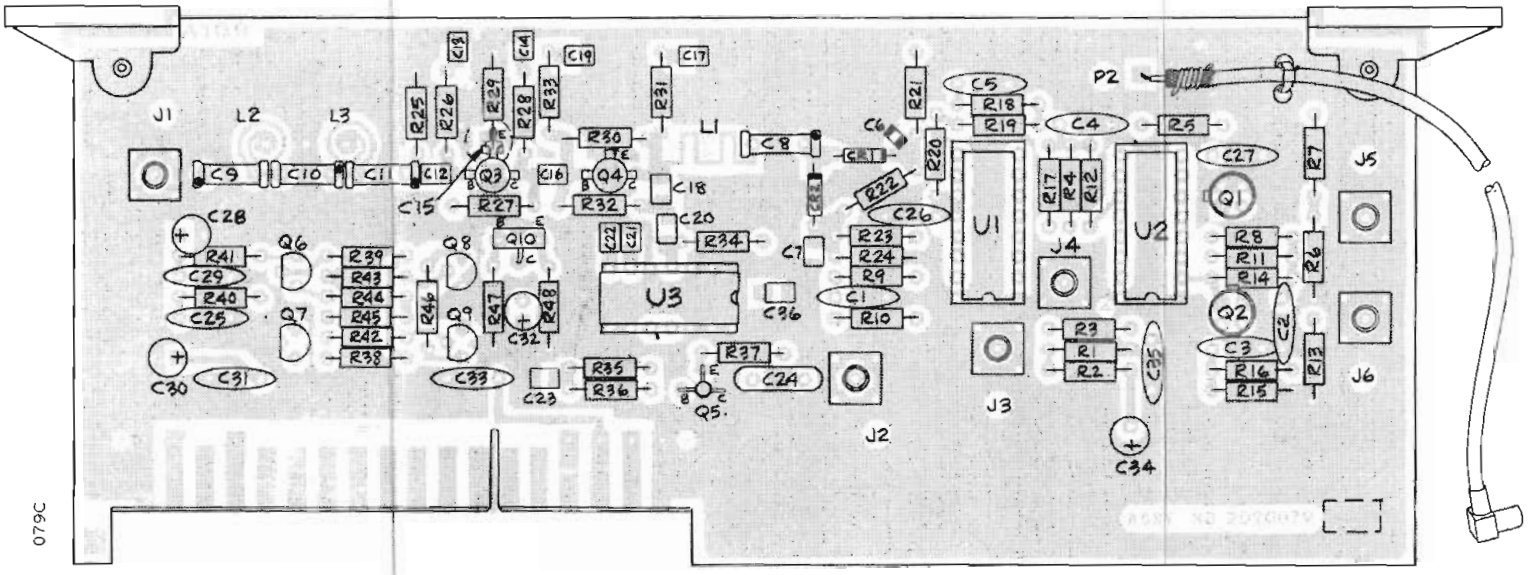
O-17. REMOTE PROGRAMMING

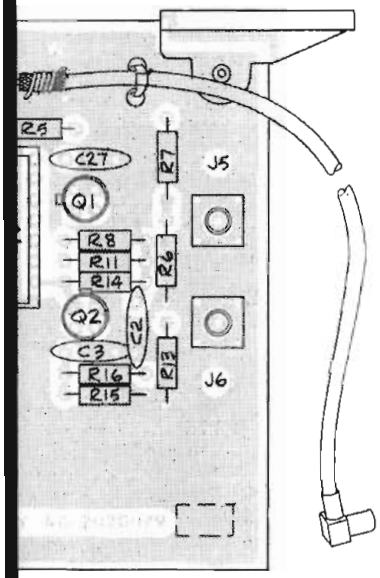
O-18. Except for POWER ON/OFF and SAMPLE RATE, all front panel switch functions can be remotely controlled. Additional remotely programmable functions which are in continuous operation and are unaffected by the status of the Local/$\overline{\text{Remote}}$ line, are: $\overline{\text{Fast}}$ Cycle, Cycle Counter, and Pulse Reset. $\overline{\text{Fast}}$ Cycle bypasses the display delay generator and over-rides the SAMPLE RATE control. Cycle Counter is a capacitive-coupled input signal to reset the Basic Counter and initiate a new reading. Pulse Reset triggers a one-shot to reset the Counter and Converter.

O-19. U6 through U9 are quad 2-input multiplexers which are selected by the Local/$\overline{\text{Remote}}$ line to provide data from either the front panel switches (Local mode), or from the rear panel connector A1J7 ($\overline{\text{Remote}}$ mode). R6-R9 and U3 act as an input buffer for the INHIBIT line, thus allowing operation from 0 to +50 volts. CR1 and CR2 act as clamping diodes.

O-20. OPTION P5 - GENERAL PURPOSE INTERFACE BUS

See manual supplement.


J1
L2
L3
L1
P2
J5
J6
J4
J3
J2
U1
U2
U3
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
079C



PRESCALER (A109)

General

This option permits the measurement of pulse modulated signals that lie within the frequency range of 300 MHz to 950 MHz, and with pulse widths as narrow as 100 nsec.

The Prescaler divides the input signal frequency by four before applying it to the High Frequency board (A106). Simultaneously, the gate time is extended by a factor of four, to allow display of the true input frequency.

Circuit Description

Input RF power is amplified in broadband limiting amplifiers Q3 and Q4, and applied to U3 which divides the frequency by four. Emitter follower Q5 provides sufficient drive current for 50 ohms lines.

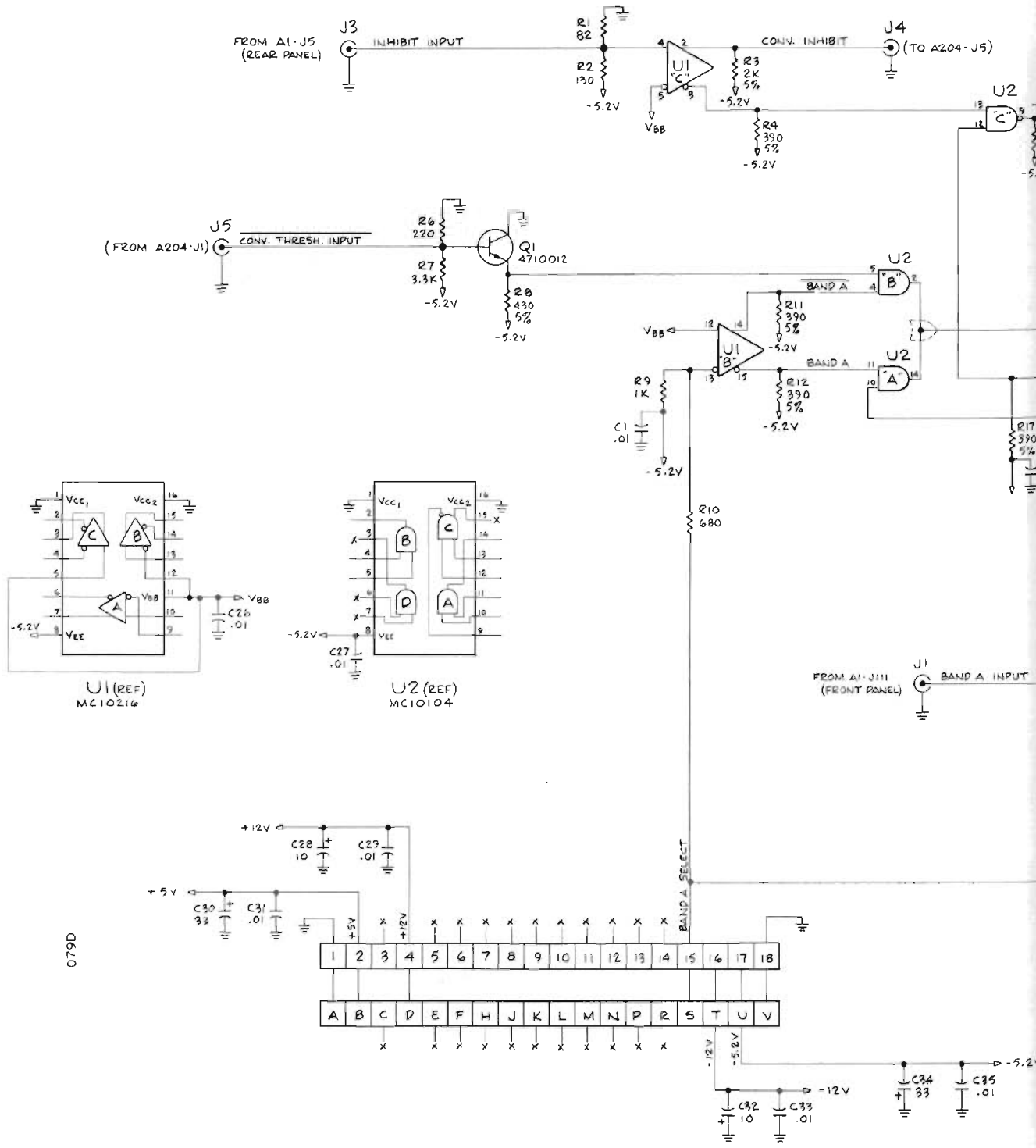
The output of Q3 and Q4 is also applied to a threshold trigger circuit. The envelope is first detected by C6, CR1, and CR2, before driving Schmitt trigger U1A. Threshold of the Schmitt circuit is adjusted to trigger only at signal levels that are sufficiently large enough to permit reliable counting in the divide by four circuitry of U3.

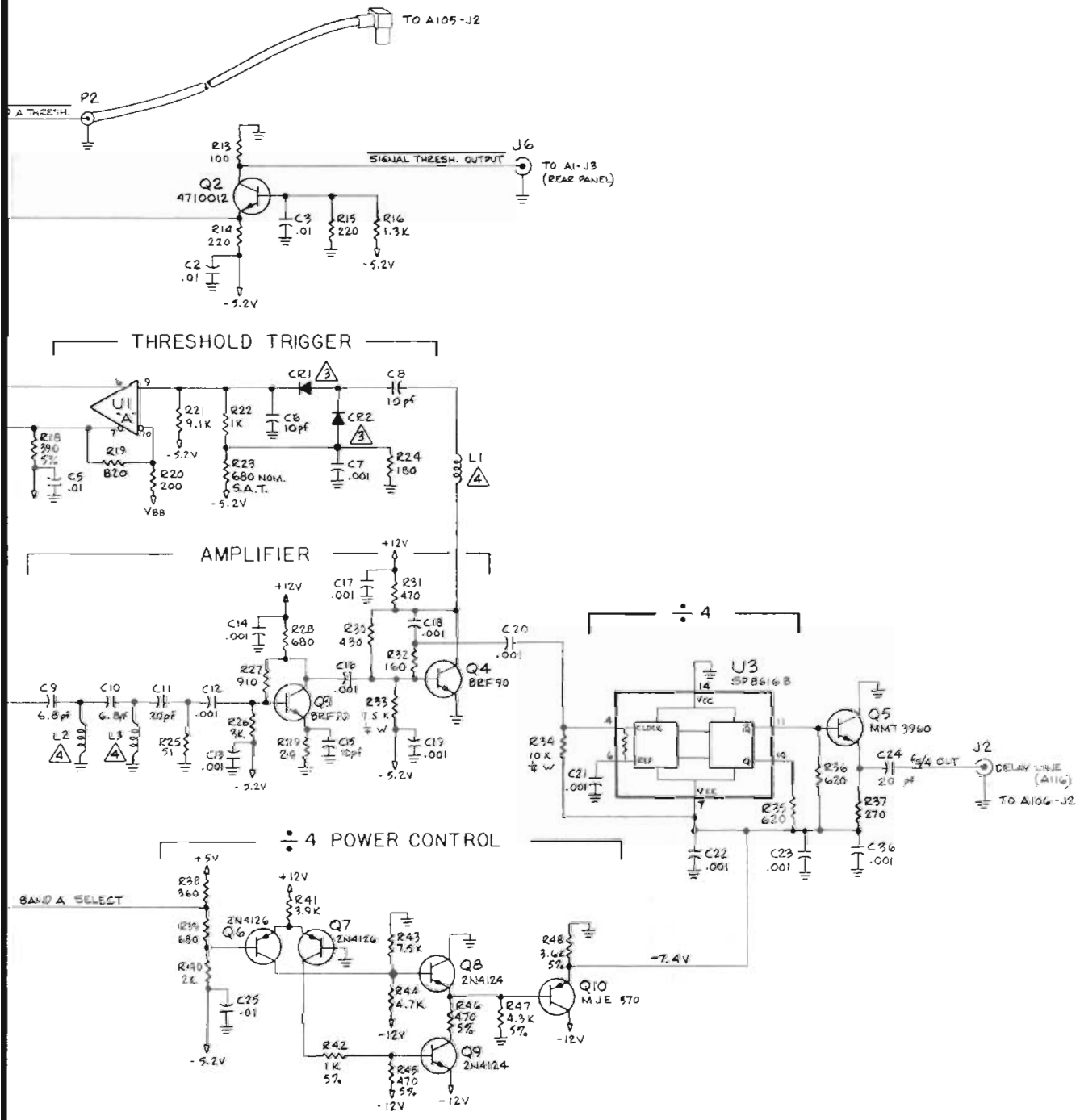
Power for U3 is switched on or off by the circuitry associated with Q6 - Q10. When the Band A Select line goes to a TTL high, differential amplifier Q6/7 saturates Q9 and allows the base of Q8 to become biased at approximately -7.4 volts. Q8 and Q10 are emitter followers that supply the -7.4 volts at approximately 60 ma to U3.

The remainder of the circuitry is interface switching logic to provide the indicated control signals. When the Band A Select line goes to a TTL high, U2A is enabled and passes the Band A signal threshold to the SIGNAL THRESHOLD output connector on the rear panel of the counter. Conversely, when the line is a TTL low, the Converter threshold signal is passed through U2B to the connector.

If the INHIBIT INPUT is either open, an ECL low (-1.7 V), or -1 volt from a 50 ohm source, U1C enables U2C allowing passage of the threshold trigger to the Gate Generator.

FIGURE P2-A
COMPONENT LOCATOR
PRESCALER (A109)
OPTION P2


FROM A1-J5
(REAR PANEL)
J3
INHIBIT INPUT
R1
82
R2
130
-5.2V
U1
"C"
R3
2K
5%
CONV. INHIBIT
J4
(TO A204-J5)
VBB
R4
390
5%
U2
J5
(FROM A204-J1)
CONV. THRESH. INPUT
R6
220
R7
3.3K
Q1
4710012
R8
430
5%
BAND A
R11
390
5%
U1
"B"
R12
390
5%
R9
1K
C1
.01
R10
680
U1 (REF)
MC10216
U2 (REF)
MC10104
Vcc1
Vcc2
VEE
C26
.01
C27
.01
FROM A1-J111
(FRONT PANEL)
J1
BAND A INPUT
+12V
C28
10
C29
.01
+5V
C30
33
C31
.01
BAND A SELECT
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
A B C D E F H J K L M N P R S T U V
C32
10
C33
.01
C34
33
C35
.01
079D

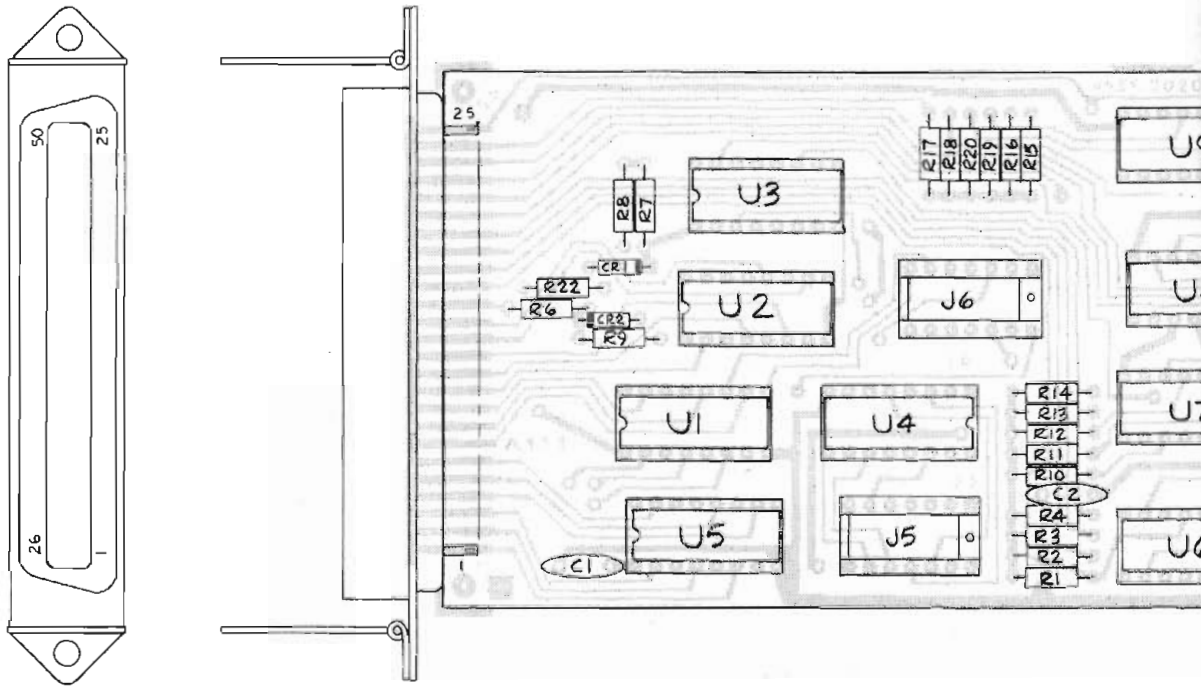


3 SEE PARTS LIST.

4 PART OF PC BOARD.

FIGURE P2-B
SCHEMATIC DIAGRAM
PRESCALER (A109)
OPTION P2

Pin No.	Function	Pin No.	Function	Pin No.	Fun
1	10^4 A	18	$\overline{\text{Preset 1 GHz}}$	35	10^8
2	10^4 B	19	$\overline{\text{Preset 0.4 GHz}}$	36	10^9
3	10^5 A	20	Conv. Man/$\overline{\text{Auto}}$	37	10^9
4	10^5 B	21	Cycle Counter	38	10^{10}
5	10^6 A	22	$\overline{\text{Fast Cycle}}$	39	+5 V
6	10^6 B	23	$\overline{\text{1 MHz}}$ Resolution	40	Pri
7	10^7 A	24	$\overline{\text{Band A}}$	41	Pre
8	10^7 B	25	Local/$\overline{\text{Remote}}$	42	Pre
9	10^8 A	26	10^4 C	43	Pre
10	10^8 B	27	10^4 D	44	Pre
11	10^9 A	28	10^5 C	45	Hol
12	10^9 B	29	10^5 D	46	Tes
13	10^{10} A	30	10^6 C	47	Res
14	10^{10} B	31	10^6 D	48	100
15	Inhibit	32	10^7 C	49	Pul
16	$\overline{\text{Preset 10 GHz}}$	33	10^7 D	50	Gro
17	$\overline{\text{Preset 4 GHz}}$	34	10^8 C		

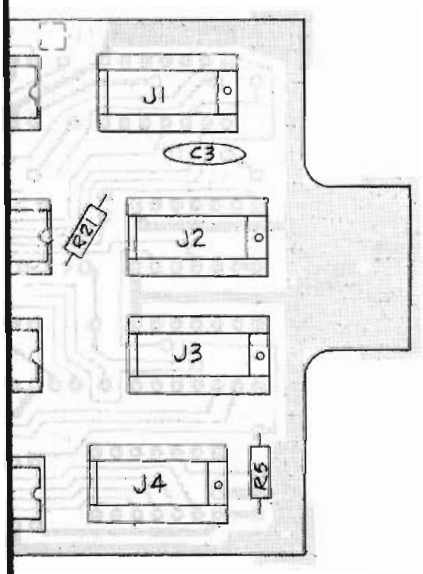


0820

NOTES FOR TABLE O-1:

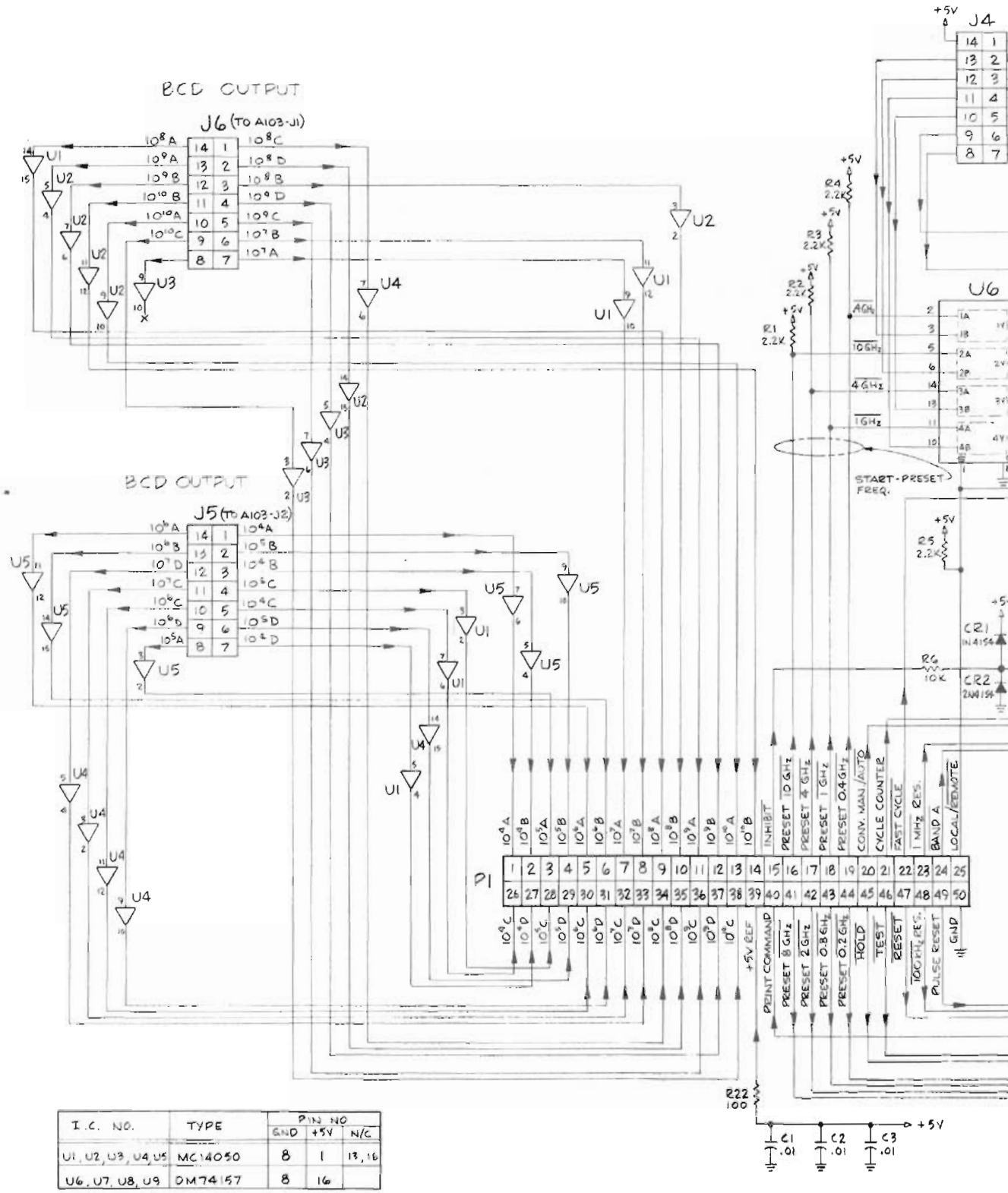
1. The 10^4 bit is the least significant bit, and corresponds to the 10 kHz output. A, B, C, and D are the 1, 2, 4, and 8 bits of each BCD digit.
2. "Barred" commands ($\overline{\text{Hold}}$, $\overline{\text{Test}}$, etc.) are active low.
3. The command "$\overline{\text{Hold}}$" retains the reading until manually reset. "$\overline{\text{Test}}$" provides the same information as the front panel **TEST** switch. "$\overline{\text{Reset}}$" over-rides the **SAMPLE RATE/HOLD** control, resets the display to zero, and initiates a new reading. "$\overline{\text{100 kHz}}$" and "$\overline{\text{1 MHz}}$" set the resolution in the same manner as the front panel **RESOLUTION** switches. "$\overline{\text{Band A}}$" places the counter in the Band A (Prescaler) range: 300 MHz – 950 MHz.

TABLE O-1
PIN ASSIGNMENTS
BCD OUTPUT/REMOTE
PROGRAMMING CONNECTOR
(A1J7)



REFER TO PAGE O-1 FOR CIRCUIT DESCRIPTION

FIGURE P4-A
COMPONENT LOCATOR
BCD OUTPUT/REMOTE
PROGRAMMING (A111)
OPTION P4



I.C. NO.	TYPE	PIN NO		
		GND	+5V	N/C
U1, U2, U3, U4, U5	MC14050	8	1	13, 16
U6, U7, U8, U9	DM74157	8	16	

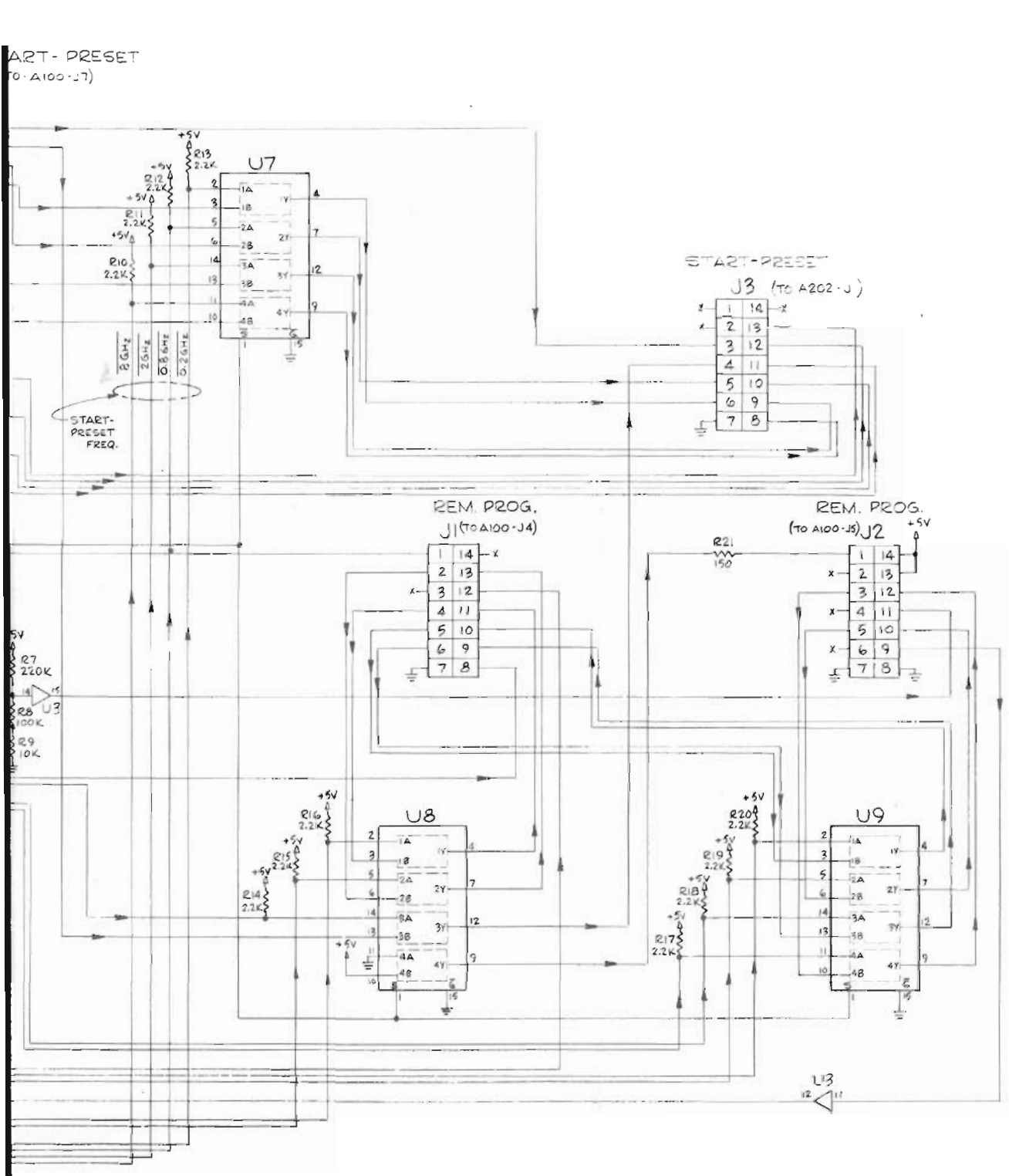
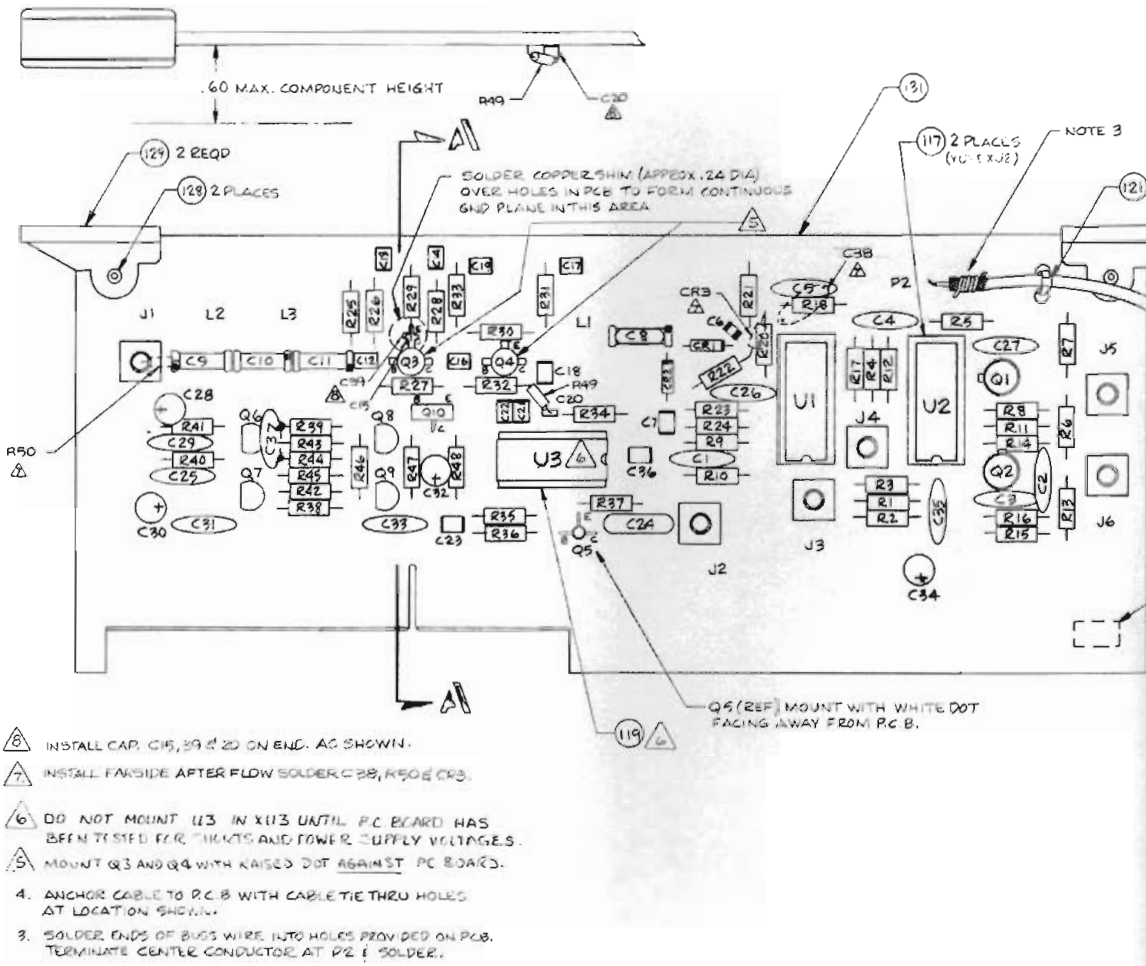
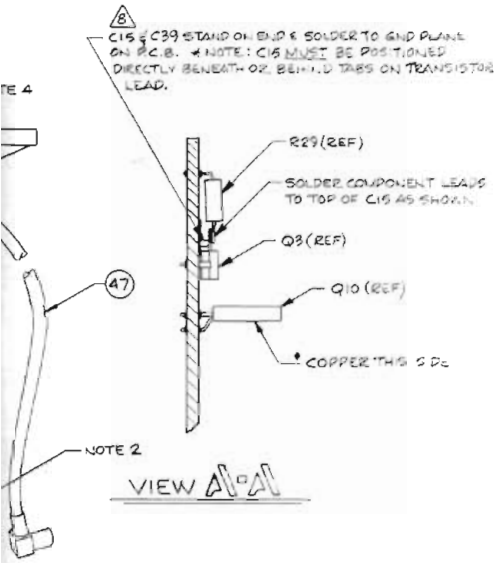


FIGURE P4-B
SCHEMATIC DIAGRAM
BCD OUTPUT/REMOTE
PROGRAMMING (A111)
OPTION P4



6. INSTALL CAP. C15, 39 & 20 ON END. AS SHOWN.
7. INSTALL FARSIDE AFTER FLOW SOLDER C38, R50 & CR3.
6. DO NOT MOUNT U3 IN X113 UNTIL P.C. BOARD HAS BEEN TESTED FOR SHORTS AND POWER SUPPLY VOLTAGES.
5. MOUNT Q3 AND Q4 WITH RAISED DOT AGAINST P.C. BOARD.
4. ANCHOR CABLE TO P.C.B WITH CABLE TIE THRU HOLES AT LOCATION SHOWN.
3. SOLDER ENDS OF BUSS WIRE INTO HOLES PROVIDED ON PCB. TERMINATE CENTER CONDUCTOR AT P2 & SOLDER.



2020079-P

PRESCALER (A109)

General

This option permits the measurement of pulse modulated signals that lie within the frequency range of 300 MHz to 950 MHz, and with pulse widths as narrow as 100 nsec.

The Prescaler divides the input signal frequency by four before applying it to the High Frequency board (A106). Simultaneously, the gate time is extended by a factor of four, to allow display of the true input frequency.

Circuit Description

Input RF power is amplified in broadband limiting amplifiers Q3 and Q4, and applied to U3 which divides the frequency by four. Emitter follower Q5 provides sufficient drive current for 50 ohms lines.

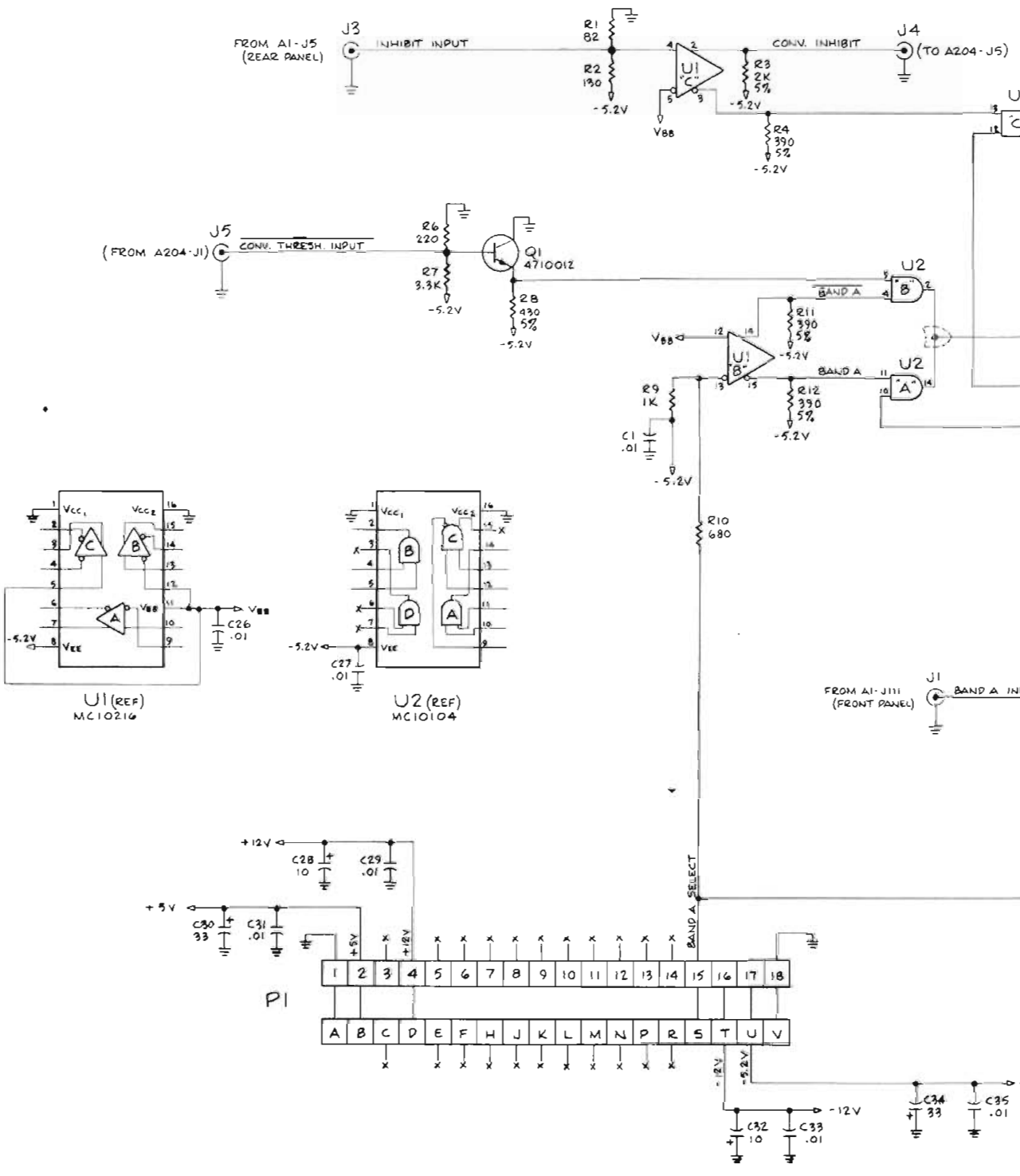
The output of Q3 and Q4 is also applied to a threshold trigger circuit. The envelope is first detected by C6, CR1, and CR2, before driving Schmitt trigger U1A. Threshold of the Schmitt circuit is adjusted to trigger only at signal levels that are sufficiently large enough to permit reliable counting in the divide by four circuitry of U3.

Power for U3 is switched on or off by the circuitry associated with Q6 - Q10. When the Band A Select line goes to a TTL high, differential amplifier Q6/7 saturates Q9 and allows the base of Q8 to become biased at approximately -7.4 volts. Q8 and Q10 are emitter followers that supply the -7.4 volts at approximately 60 ma to U3.

The remainder of the circuitry is interface switching logic to provide the indicated control signals. When the Band A Select line goes to a TTL high, U2A is enabled and passes the Band A signal threshold to the SIGNAL THRESHOLD output connector on the rear panel of the counter. Conversely, when the line is a TTL low, the Converter threshold signal is passed through U2B to the connector.

If the INHIBIT INPUT is either open, an ECL low (-1.7 V), or -1 volt from a 50 ohm source, U1C enables U2C allowing passage of the threshold trigger to the Gate Generator.

FIGURE P2-A
COMPONENT LOCATOR
PRESCALER (A109)
OPTION P2



L1, L2 & L3 ARE PART OF P.C. BOARD.

CR1 & CR2 ARE HP P/N 5082-2835.

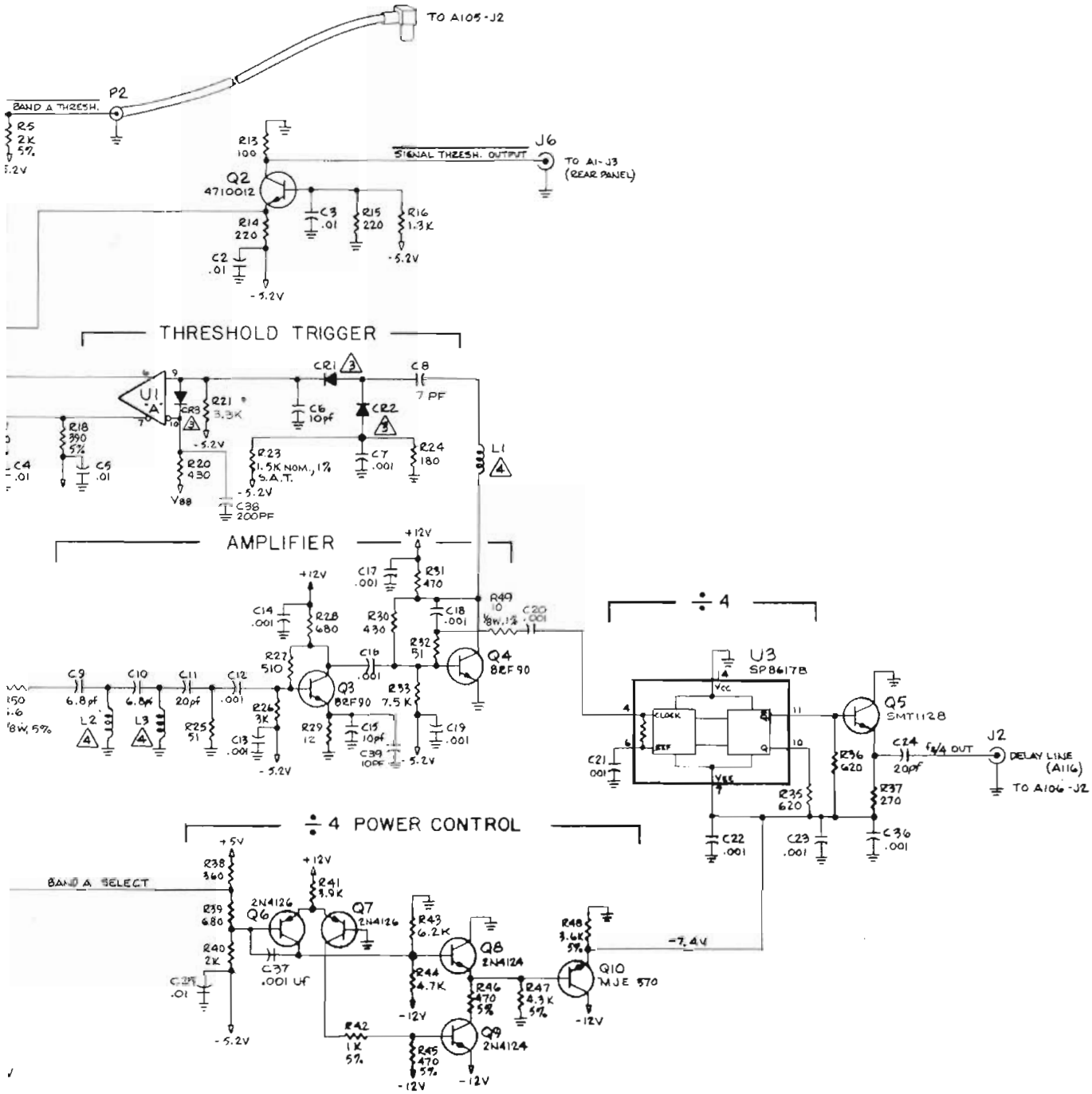


FIGURE P2-B
SCHEMATIC DIAGRAM
PRESCALER (A109)
OPTION P2

MANUAL CHANGE INFORMATION
MODEL 451

THE FOLLOWING CHANGES APPLY TO THE V-11 MODIFICATION OF A BASIC COUNTER AND DO NOT INCLUDE OTHER CHANGES DUE TO THE ADDITION OF OPTIONS OR OTHER MODIFICATIONS.

IN ANY CORRESPONDENCE OR PARTS ORDERING RELATED TO THIS COUNTER, BE SURE TO SPECIFY THE COMPLETE MODEL AND SERIAL NUMBER OF THE COUNTER.

DESCRIPTION :

V-11 modifies the 451 counter so it can accept a 50 - 400 Hz power input.

MODIFICATION :

Removal of the standard fan and installation of a 24 VDC fan (part number 5000065). The fan connection is modified so that its power is taken directly from the power supply board.

MANUAL CHANGES :

Change the Specifications on page 1-2 to read :

POWER : 100/120/220/240 VAC + 10%, 50 - 400 Hz, 100 W nominal

Change paragraph 2-5, on page 2-1, to read :

100/120 or 220/240 volt, 50 - 400 Hz power, etc.

JUNE 12, 1980

MANUAL CHANGE INFORMATION

MODEL 451

At EIP we continually strive to keep up with the latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipment requirements, we cannot get these changes immediately into printed manuals. As a result, your instrument may contain some or all of the changes listed below.

PAGE NUMBER:

0-3. A109 Prescaler (5500079), Change R33 to 7.5K, 1/4 W.
Change R34 to 10K, 1/4 W.

0-5. A111 BCD Output/Remote Prog., Signal from P1 pin 15 to R6 should be inhibit.

3-1. Paragraph 3-8, line 4, should read "925 MHz - 18 GHz, or Band A (Option P2) for frequencies".

3-1. Paragraph 3-15, last line should read "produce 1.5V at the INPUT INHIBIT thus enabling the 451".

8-7. A1 Basic Counter, Change FAN part number to 5000151.

8-7. A104 Control (2020074), Change C5 to Mica, 200 pF, part number 2250009.
Add CR18, General Purpose diode, part number 2704154.
Delete R20.

8-8. A107 Power Supply (2020077), Change C1 to part number 2200016.
Change C5 to part number 2200018.
Change C12 to part number 2200016.
Change C17 to part number 2200025.
A106 High Frequency (2020081), Change R47 to part number 4130999.

8-9. A107 Power Supply (2020077) Change R20 to part number 4130999.

8-9 A109 Prescaler (2020079) Change R33 to 4130752.
Change R34 to 4010103.

9-5. A100, (5500070) Rear panel MIN PRF switch should be labeled 0 (not ON) and 50 Hz (not OFF). The blue and green wires from J1 should be transposed so the green wire goes to 0.

9-9. A103 Count Chain schematic (5500083-A) U16, U17, and U18 - change pin 14 to pin 1.

9-13. A104 Control (5500074-D), Change C5 to 200 pF.
Replace R20 with CR18 (anode side to ground).
C2 should be 6.3 V.

9-15. A105 Gate Generator, Signal from P1M to U14C pin 2 should be clock inhibit.

9-19. A107 Power Supply (5500077), Change C1 value to 9500 uF .25V.
Change C5 value to 44,000 uF .15V.
Change C12 value to 9500.
Change C17 value to 10,000.
Change R20 to 5.6K, 2%.

9-33. A203 Converter Sequencer schematic - delete line between U7 pin 3 and U9 pin 2.
-add line between U9 pin 2 and U4 pin 1.
-change Q3, now shown as NPN, should be PNP.
-change C4 to .005 value.

4-1. Paragraph 4-4, line 6 should read " 100μs (or 1 ms)."

8-12. A204 IF Processor (2020094) - Note the following part number changes.

C25 is 2150003	R41 is 4130151
C33 is 2150003	R43 is 4130431
R32 is 4130431	R44 is 4130221
R34 is 4130271	R76 is 4130471
R35 is 4130221	

OVER

9-35. A204 IF Processor (5500094) - Change the revision letter to J and make the following changes to your schematic diagram.

C25 is now .01μF
C33 is now .01μF
R33 is now 430 ohm, 2%
R34 is now 270 ohm, 2%
R35 is now 220 ohm, 2%
R41 is now 150 ohm, 2%
R43 is now 270 ohm, 2%
R44 is now 220 ohm, 2%
R76 is now 470 ohm, 2%

1-2. Table 1-1. Specifications, General. Gate error (max) should read "$\frac{\pm 100\ kHz}{PW - .03}$" for Band A and "$\frac{\pm 40\ kHz}{PW - .03}$" for Band B.

6-5. Paragraph 6-21, item b., (3) should read "Adjust A106R60 per paragraph 6-21a (2)."

7-1. Paragraph 7-10, C. (5), last sentence should read "For 100 ns wide pulses, error should be less than 1.42 MHz.

7-2. Paragraph 7-10, D (5), last sentence should read "For 100 ns wide pulses, error should be less than 1.42 MHz.
Paragraph 7-11, C, add the following sentence, "Gate error should be less than 570 kHz.

9-5. A100 Counter Interconnect (5500070) - Delete Gate Mod switch that was connected to J1 pin 1 and 2 on the rear panel. Delete modulation trace that runs from J1 pin 1 to High Frequency XA106 pin 15.

9-15. A105 Gate Generator, J1 should read $\overline{\text{BAND B THRESHOLD}}$ and J2 should read $\overline{\text{BAND A THRESHOLD}}$.

9-17. A106 High Frequency, R47 should be 18 ohm nom., 2%, S.A.T.

9-29. A202 YIG Control, Add U8 Inverter Gate , pin 11 (in)/10(out) from P1 pin 7, 40 kHz Clock signal to U4 pin 14.

$\overline{\text{ERROR DAC ENABLE}}$, at U6 pin 2 should be ERROR DAC ENABLE.

$\overline{\text{ERROR DAC STEP}}$, at U6 pin 11 should be ERROR DAC STEP.

9-14. A105 Gate Generator, Paragraph 2 title should read "Gate and Enable Flip-flop (U2A/B)."
Paragraph 4, line 8 should read "the Time Base Flip-flop (U2B)."
Paragraph 5 title should read "Time Base Flip-flop (U3B)"

9-33. A203 Converter Sequencer, U3 (shown in two places) should be drawn as a AND gate.

8-11. A202 YIG control, Q2 should be part number 4710022.

8-4. Delete 2710030.

5-13. Top right (Yig Driver) should read "Remove A201J1."
Top left (2nd box) should read "check for ramp at A201FL1."

0-4. Pin/function table - function for pin no. 46 should read $\overline{1\ ms}$.

0-5. P1, pin 46 should read $\overline{1\ ms}$.

8-12. A204 IF Processor (2020094), Change C33 to S.A.T.
Change Q5, Q6, Q7, Q8 to part number 4710026
Add C49, Cer, .01 uF, part number 2150003

9-35. A204 IF Processor (5500094), Change C33 to S.A.T.
Change Q5 thru Q8 to type NE73432B
Add C49 between R55 and ground.

8-8. A106 High Frequency (2020081) — Q6, Q7 are now SMT1128 type transistors, part number 4710035.
Mark schematic, part number 5500081, on page 9-17.

8-12. A203 Converter Sequencer (2020093) - R35 is now part number 4010569

9-9. A103 Count Chain (5500083-A) - U20 and U21 should be type DM74LS196.

1-2. Table 1-1. Specifications, General, Pulse Characteristics; Pulse repitition frequency should read: Maximum 2.5 MHz. Add: Minimum time between pulses is 300 n sec.